Update on continuous digitization prototype tests

N. Felt, J. Oliver
30 Jan 2005

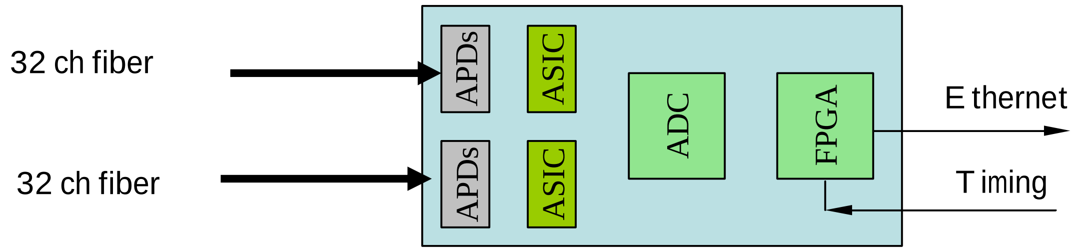
What is being tested?

- Architecture which allows for digital (as opposed to analog) processing of integrated charge signals

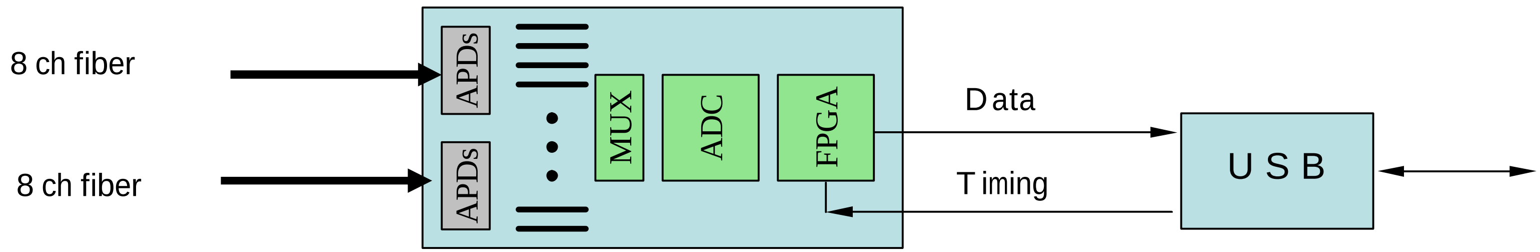
Motivations

- Deadtimeless operation
  - Allows for supernova signal detection (so long as the the detector does!)
  - Beam spill timing signal not required (although possibly useful for background rejection)
- Enhanced signal to noise
  - ~ 25% SNR improvement over DCS for same front-end (preamp)
  - ~3-5 x timing resolution improvement over raw 500ns timing bins.

Model of front end board



Prototype board under test



(both LVDS)

- Hybrid preamps in lieu of ASIC
- External multiplexer
- 16 channels / board

Features

- Single 10-bit ADC runs at 24 MS/sec (~42ns)
- Every 1/12th sample used per channel for pulse height and timing reconstruction in FPGA (500ns)
- All FPGA i/o is LVDS
- Preamp/shaper
  - Risetime constant : ~400ns (adjustable)
  - Falltime constant : Long →several 100us.
  - Sensitivity : High ~85mv/fc (adjustable)

Test – 1

- Corruption of analog signals by digital activity from ADC & FPGA
    - ➢ Run ADC continuously (MUX not running)
    - ➢ Trigger FPGA readout ~ 1kHz
    - ➢ FPGA sends (dummy) LVDS data onto output cable. Dummy data are identical for each trigger.
    - ➢ Observe output of addressed preamp / shaper & neighbors on scope. Average over many pulses to observe coherent feedthrough.

Results

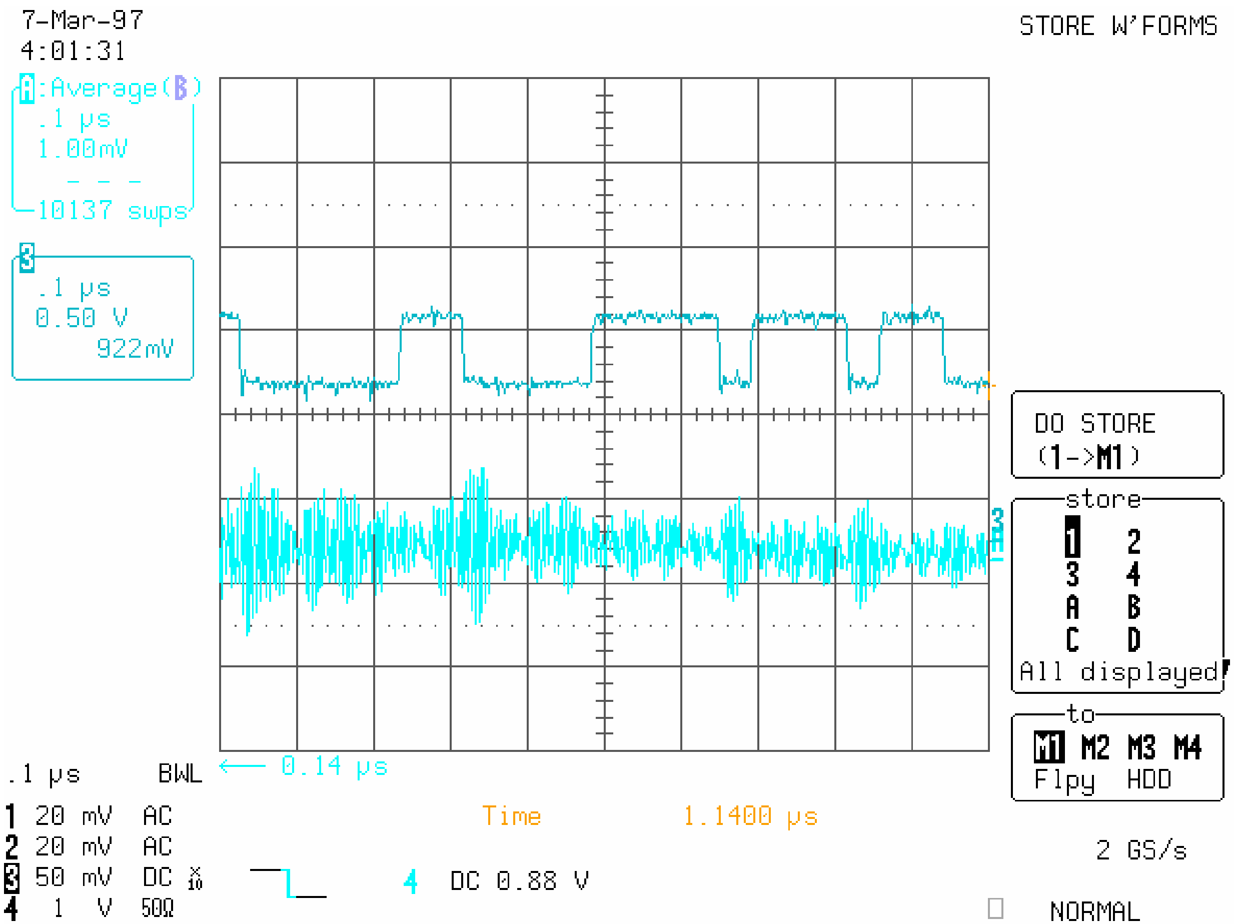
➢ Coherent noise is observable at the level of ~0.5mv rms or ~35e rms

➢ To first order, coherent noise is rejected by digitization process.

Conclusion

With care, continuous digitization is sufficiently quiet.

Digital feedthrough to preamp / shaper output

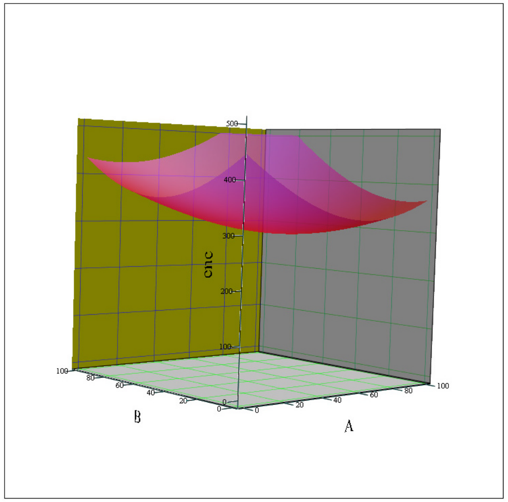


Test – 2

- Noise reduction
  - Use three pairs of DCS data
  - Separation in time = 1us, 2us, 3us
  - Combine pairs with three coefficients subject to normalization constraint

$$\alpha_1+\alpha_2+\alpha_3=1$$

  - 2-dimensional parameter space
  - Choose optimal parameters experimentally (enc minimum)

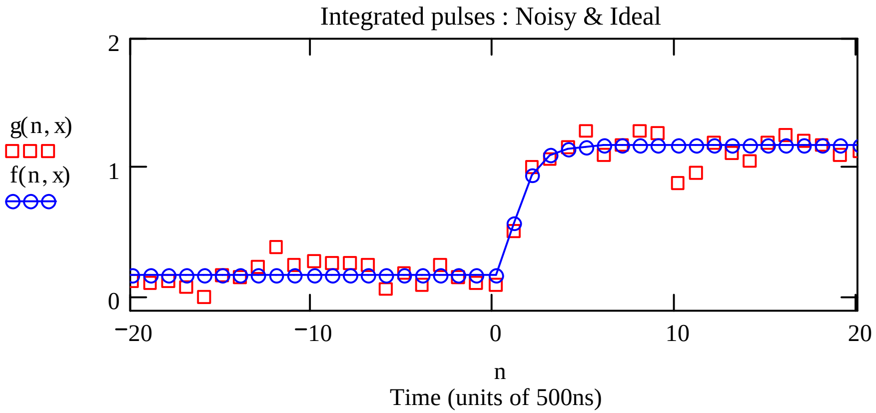


Enc

- ENC vs. 2 free parameters
- Data taken through ADC & FPGA
- ~ 25% improvement over DCS (Its not dramatic, but it's free)

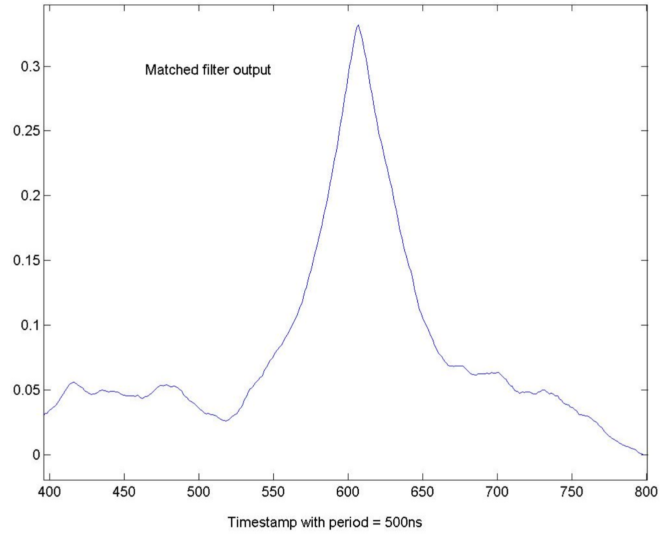
Test – 3

- Timing resolution studies (N.Felt)
  - With 500ns samples, doing nothing gives us 500ns / SQRT(12) = ~ 150ns rms
  - Test various DSP algorithms for timing improvement.
  - Scintillator decay time constant statistics (10s of ns?) not yet in model.



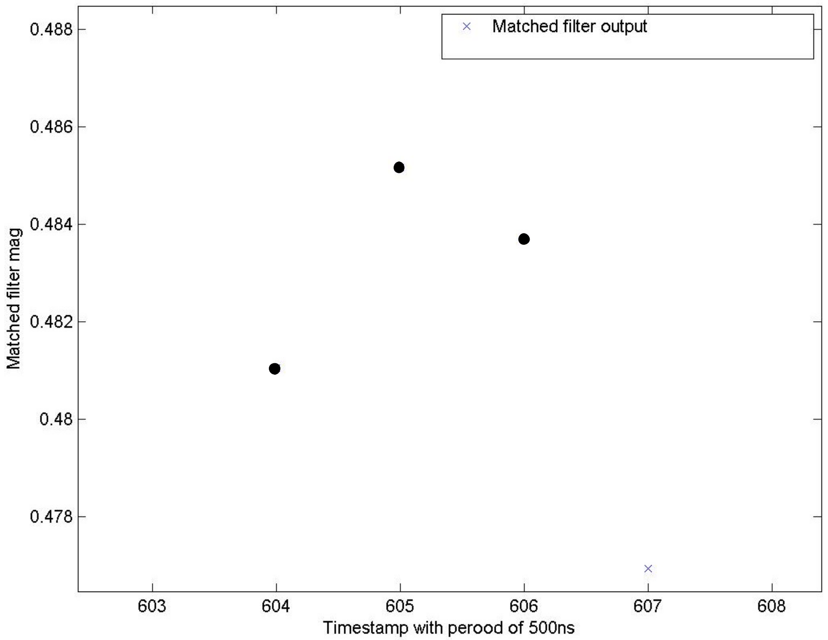
Step 1

- Apply "Matched filter" : Autocorrelation between input signal and "ideal" signal (Shown below in units of sampling time:500ns)



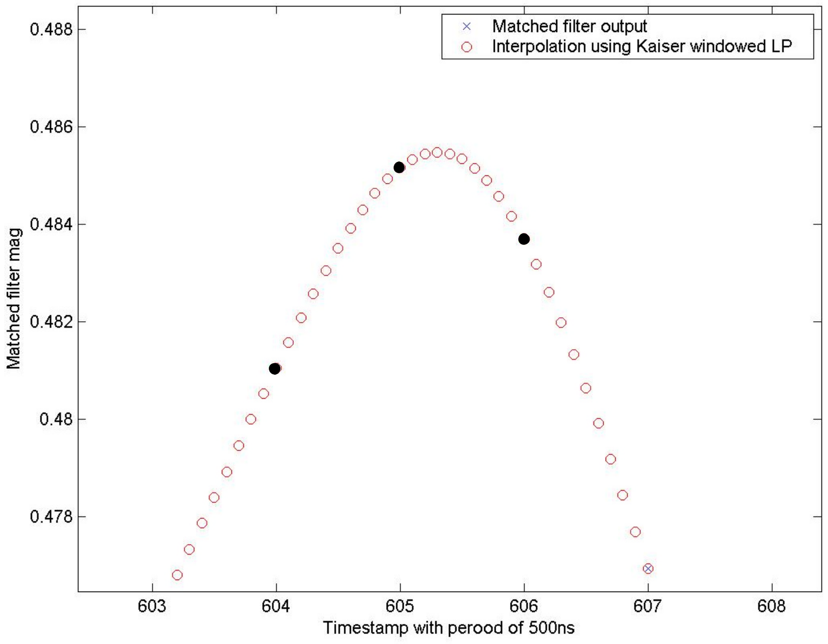
Step 2

- Interpolate between samples using sinc function (sinc(x)=sin(x) / x (Shannon's interpolation theorem)
- In example below, interpolation is 10:1 (50ns point)



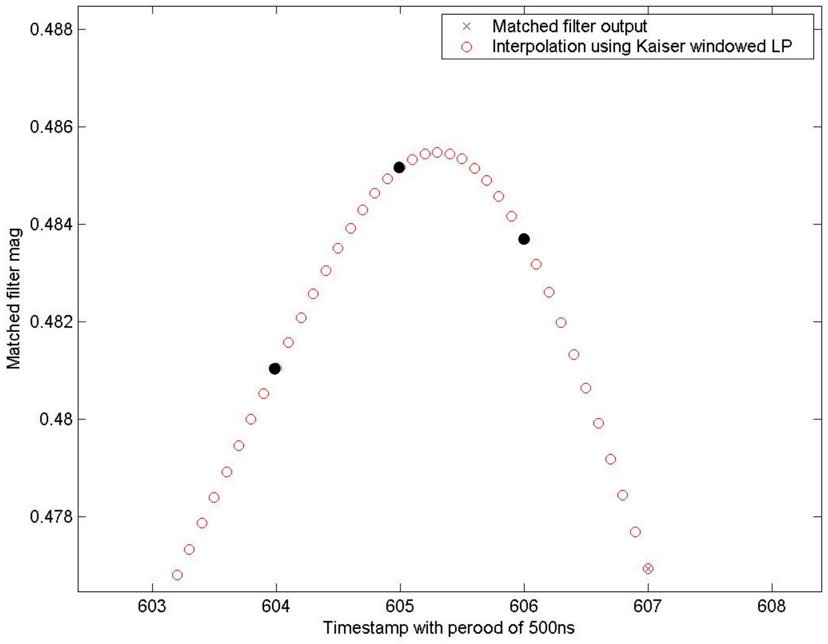
Step 2

- Interpolate between samples using sinc function (sinc(x)=sin(x) / x (Shannon's interpolation theorem)
- In example below, interpolation is 10:1 (50ns point)



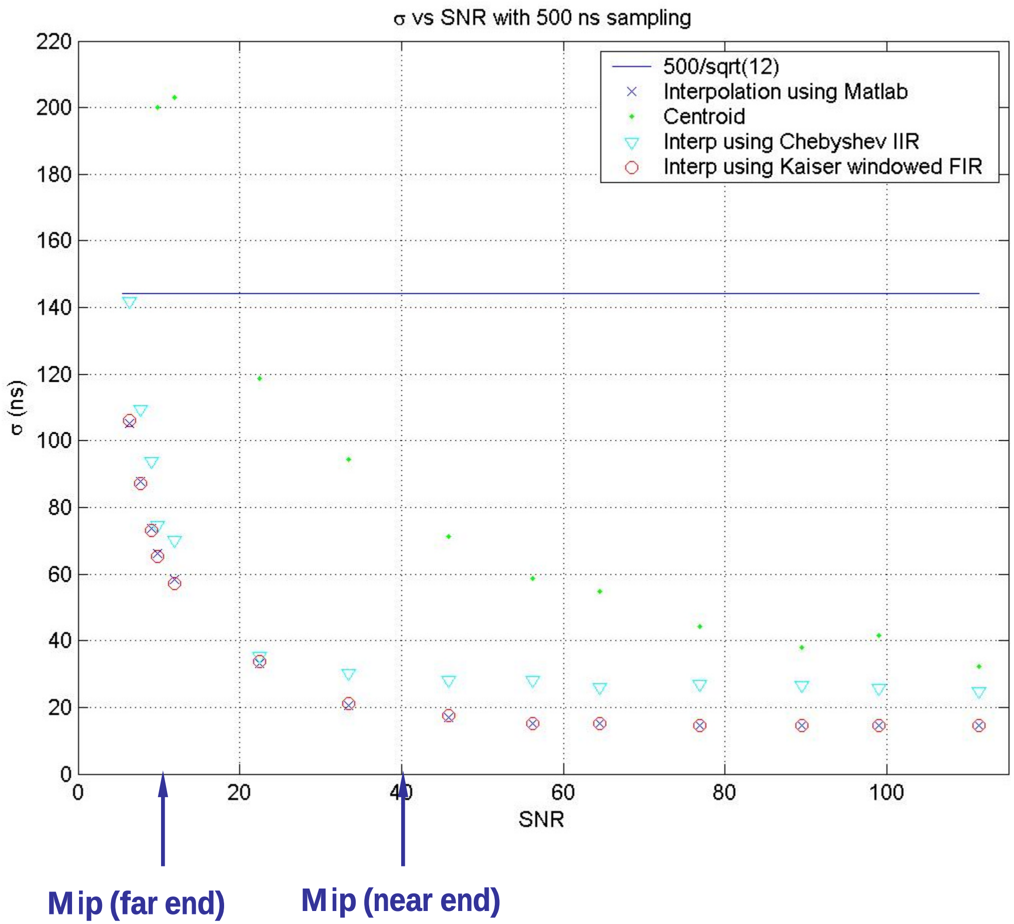
Step 3

- Extract "time" from peak of interpolated matched filter output.
- Simplest: Choose tallest sample
- Centroid would likely do better.



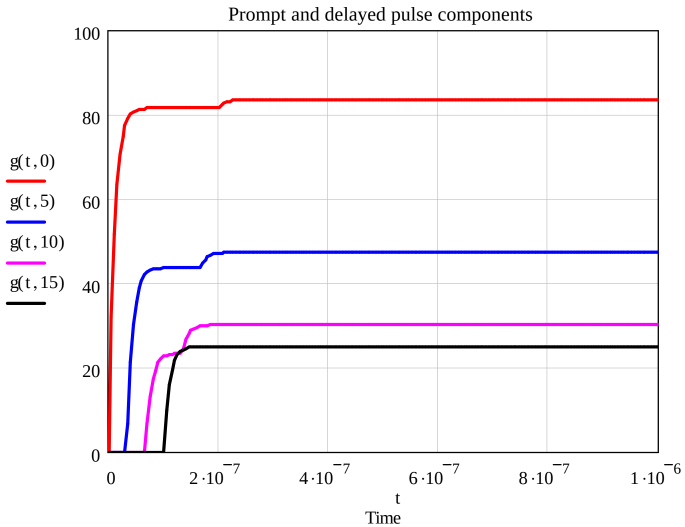
Results

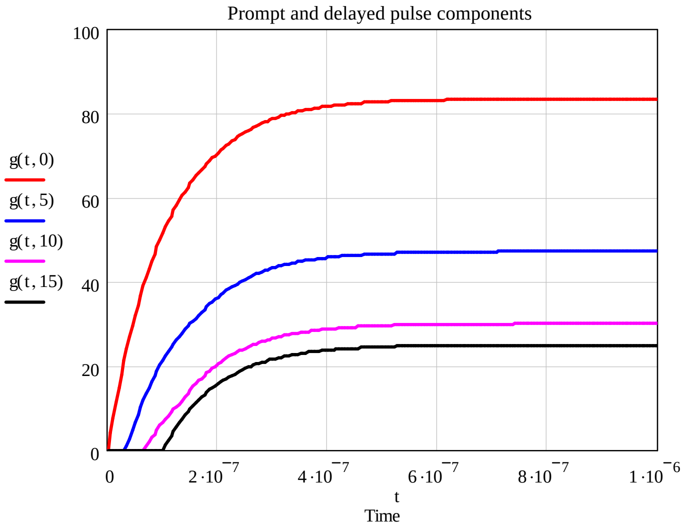
- Tallest sample algorithm (various interpolation methods)



Pulse shape issues

- A P D always sees two pulses; the prompt and the delayed components
- T his is visible for fast pulse shaping (shown here at 10ns risetime constant
- It washes out at anything more than 100ns or so (as shown here)
- N ot an issue since risetime >> total fiber delay: S hould not affect timing resolution





Conclusions

- Quiet continuous digitize / read is possible
- Deadtimeless operation possible (but not essential)
- Operation without Beam Trigger possible
- Low data rate environment
    - On-chip Dual Correlated Sampling is not required & is too restrictive
    - Collect all digitized samples
    - Improved SNR (~25%)
    - Improved timing resolution (3x – 5x)
    - Improvements dependent on noise spectrum (preamp) – can be optimized in-situ (FPGA firmware)
    - Improvements are <u>free</u>