
Update on APD's and Front End Electronics

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Progress

- ◆ *Discussions with Hamamatsu on APD layout.*
 - Progress with common understanding.
 - Questions for us to address.
- ◆ *Tom Zimmerman has completed his design and simulation of an ASIC for the APD readout.*
- ◆ *New results from the Harvard group front-end design and prototype.*
- ◆ *Some thoughts on cooling schemes.*

Current Straw Man concept.

- ◆ *32-channel's per APD - module.*
 - Complexity with combining several APD dies in the same system with TE coolers etc.
 - Matched to 32-channel detector modules. (?)
 - Preferred number of channels for Tom Zimmerman ASIC design – no special advanced technologies required.

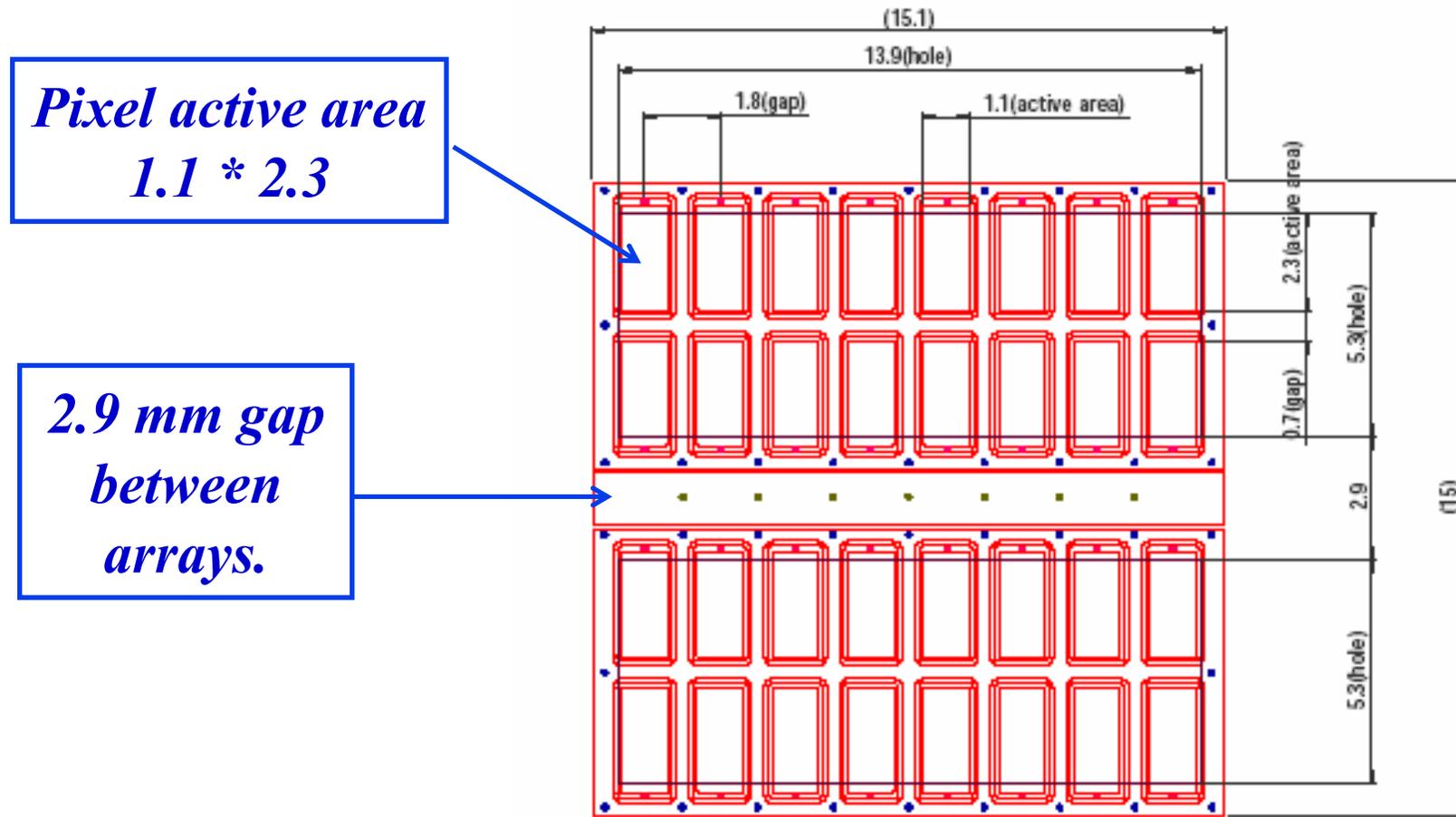
This is really a straw man concept and nothing is set in concrete.

Discussions with Hamamatsu

◆ *APD layout.*

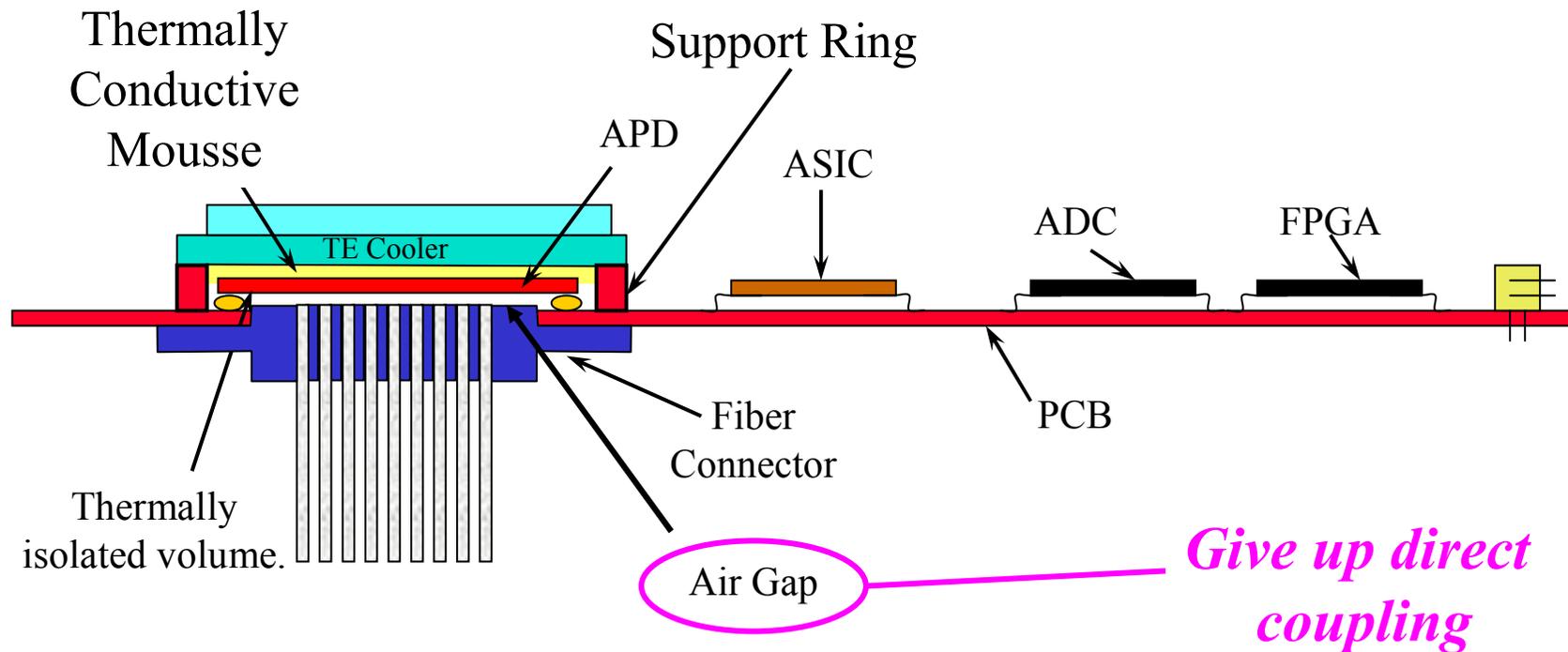
- They proposed a 4 by 8 array to us.
- It had a row of solder bumps along the middle to bring out the signal and to provide mechanical support.
- Requested preferences on three options:
 1. One 2 by 16.
 2. Two 2 by 8's on separate dies.
 3. Two 2 by 8's on a single die.
- Preference is for 3.

APD layout



Is the gap wide enough for the fiber connector?

Discussions with Hamamatsu 2



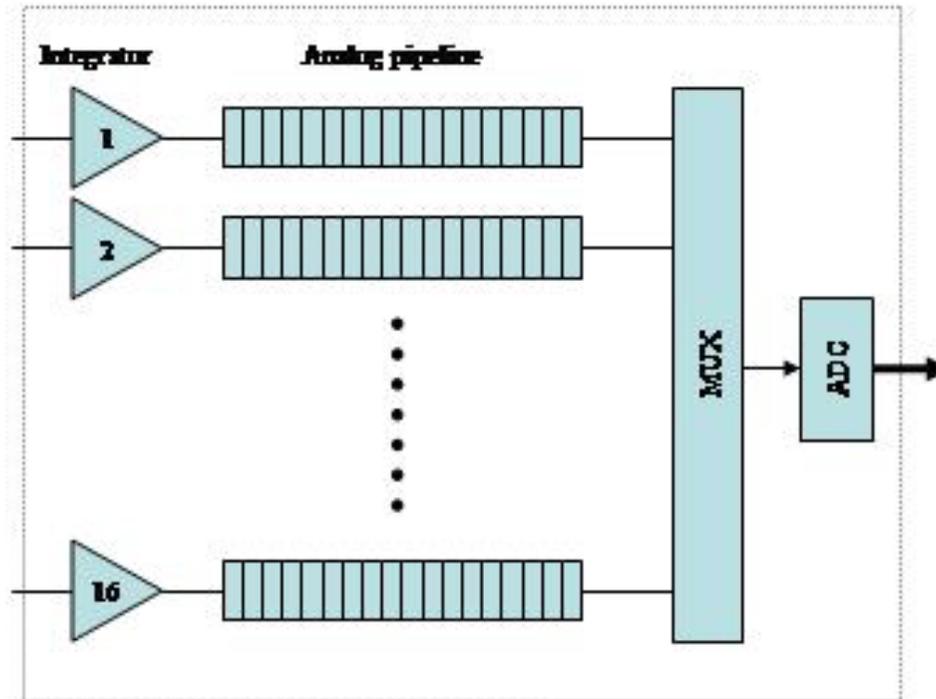
*Current detector model with Hamamatsu.
All other options have been dropped.*

Other options are being thought through see talk by Jon Urheim

Front-End Readout options.

- ◆ *Two options have been considered for the design of the front-end readout the APD.*
- ◆ *Harvard design – see talk by John Oliver later.*
- ◆ *Tom Zimmerman has designed a version of the front-end ASIC.*

New Design

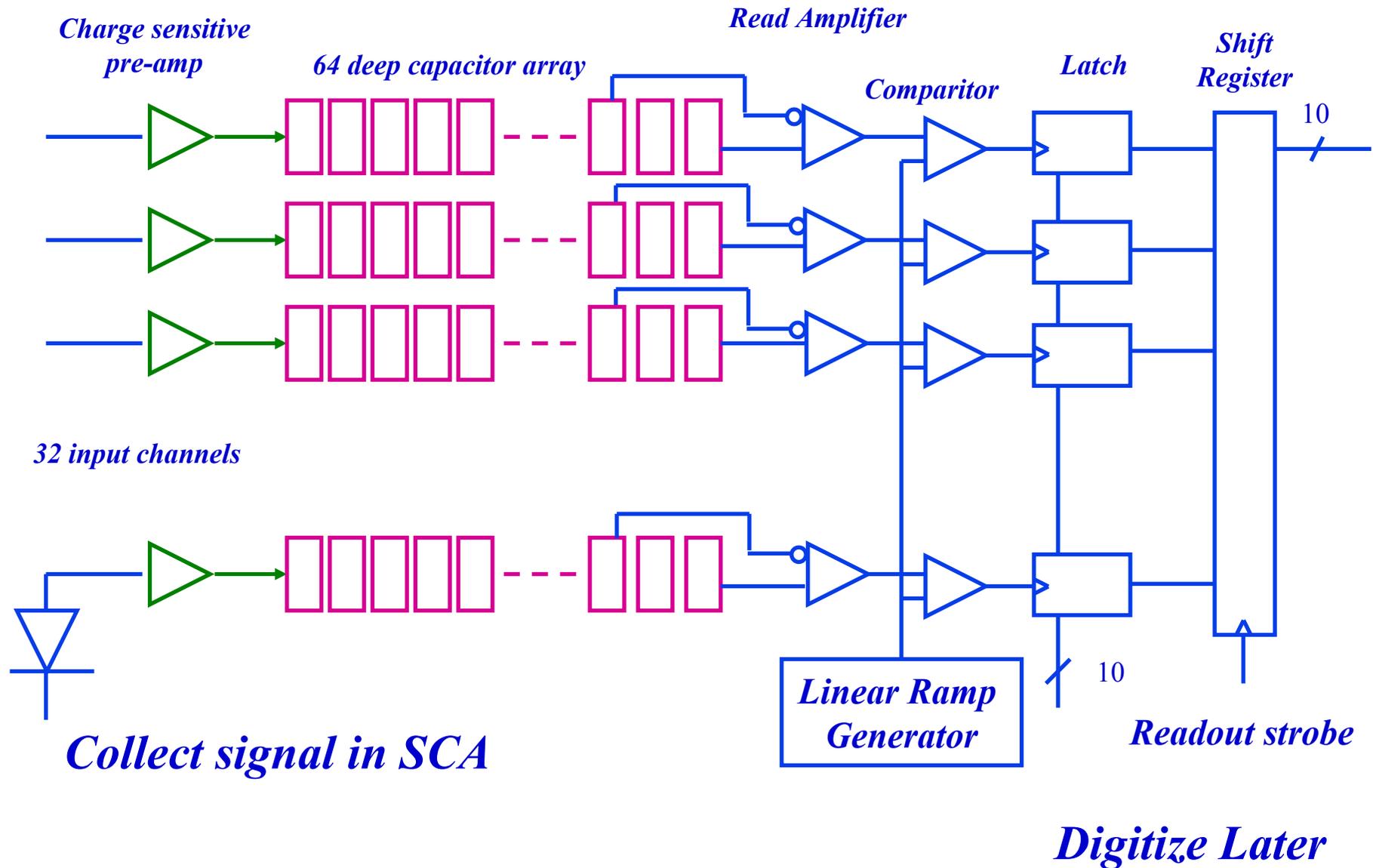


Basic design that is an extension of the MASDA approach.

Basic Concept

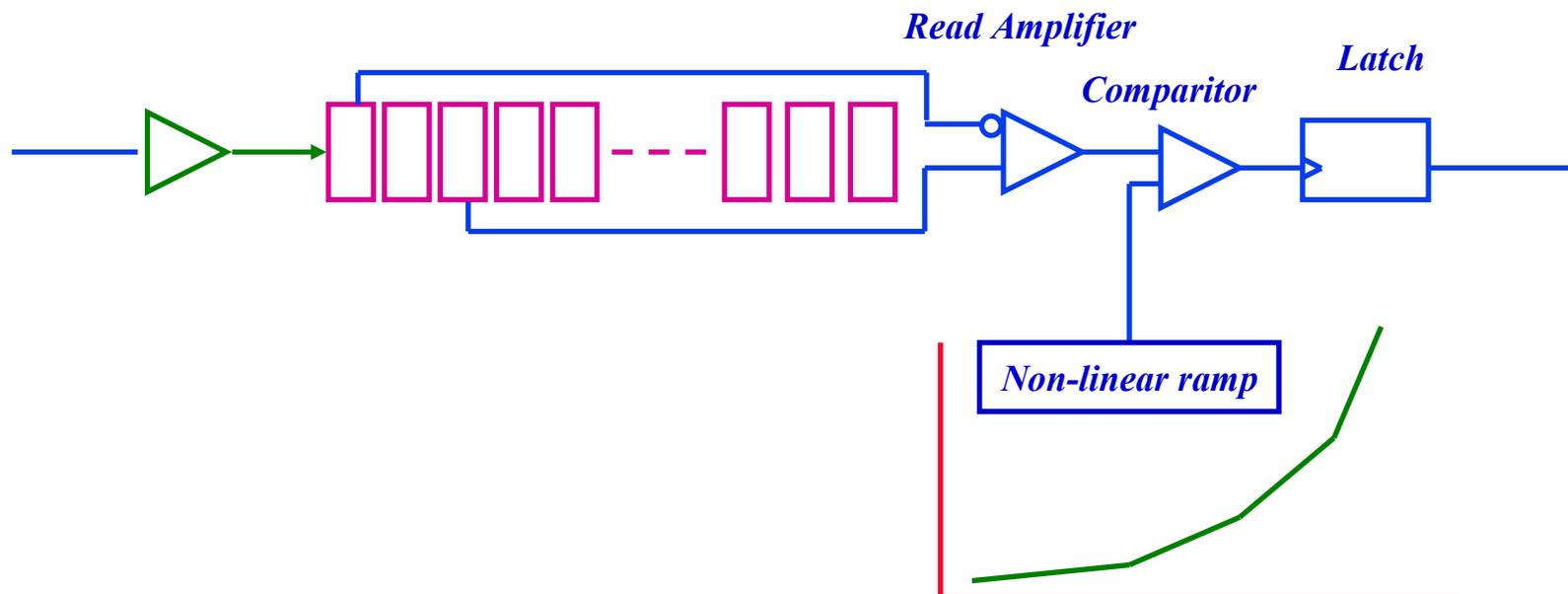
- ◆ *Optimize design for low-noise readout during the spill.*
 - 32-channels
 - Track and hold amplifier which is sampled every 500 nsec for 30 microseconds to cover spill. Samples are stored in a 64 deep switched capacitor array (64×32).
 - After spill begin conversion process.
 - » 32 channels compared with linear ramp. 10-bit resolution.
 - » Covert next ramp and send out data.
 - » Repeat until all channels digitized.
 - Digitize difference between odd neighbor cells OR digitize each cell and subtract digitally.

Main Operation – Precision Mode



Alternative Operation – Fast Digitization Mode.

- ◆ *Variants on the standard operation are included in the design.*
 - Direct in to latch.
 - Non-linear ramp.
 - Complete digitization in 400 nsec.



Proposed Operation

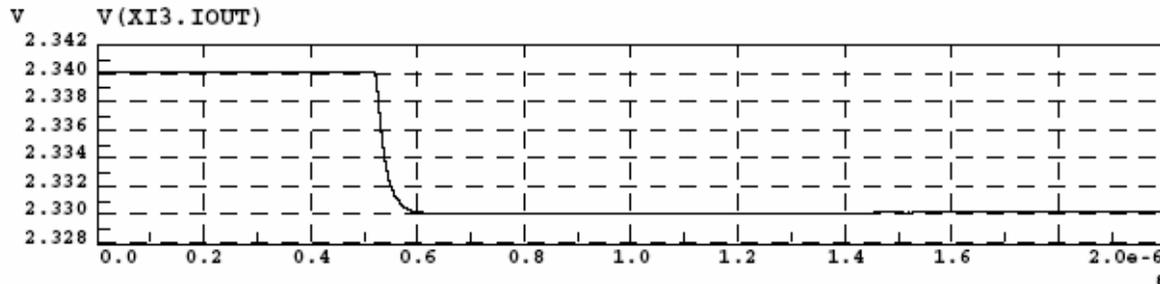
- ◆ *Run in precision mode during spill.*
- ◆ *At end switch to fast digitization mode. Collect for supernova events.*
- ◆ *Before next spill switch back to precision mode.*

Allows high precision sampling of beam events and high speed readout of small signals that are expected in SN events.

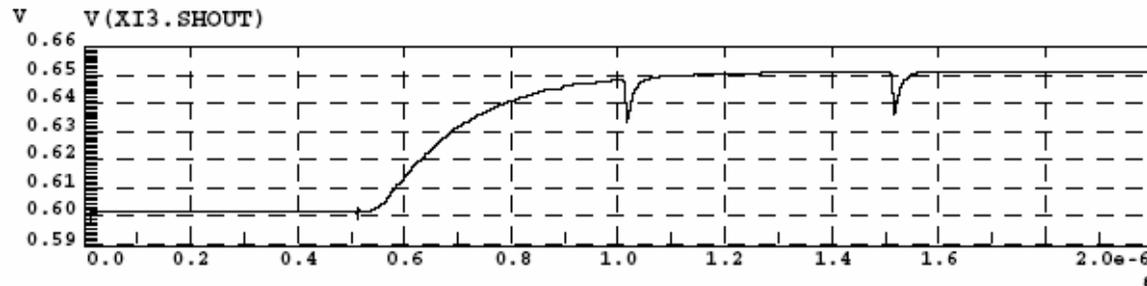
Status

- ◆ *Design complete.*
- ◆ *Full simulations complete. Calculated noise level with 10 pf and 250 nsec shaping is 150 electrons. Reality: hope for expect ~200.*
- ◆ *Next step layout and produce short run in 0.25 μ process. This will wait until design choice and funding decision.*

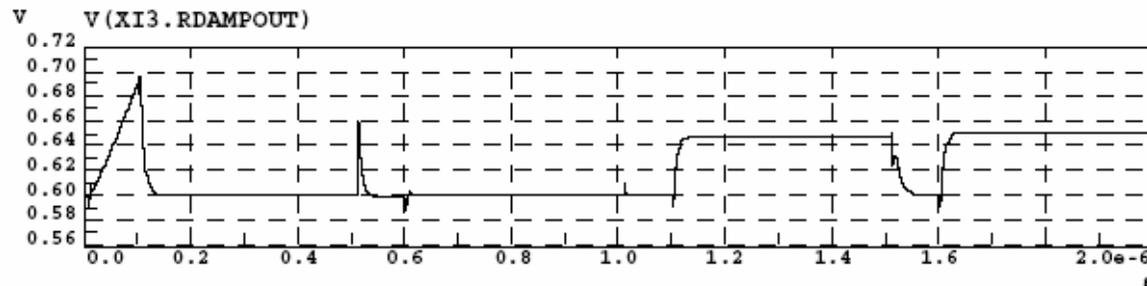
Simulations



Integrator

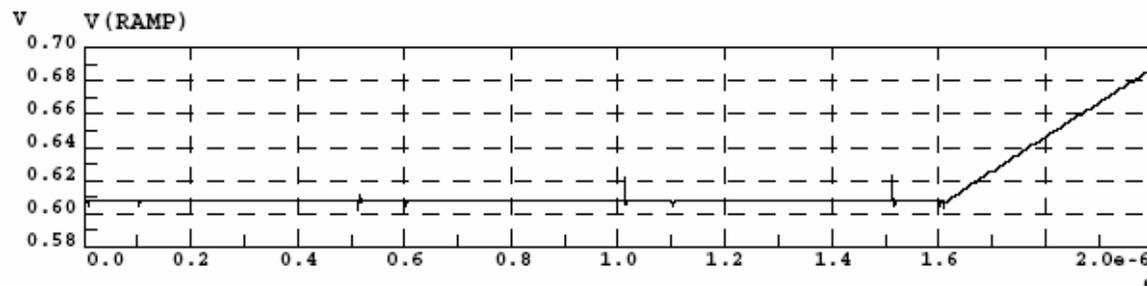


Shaper



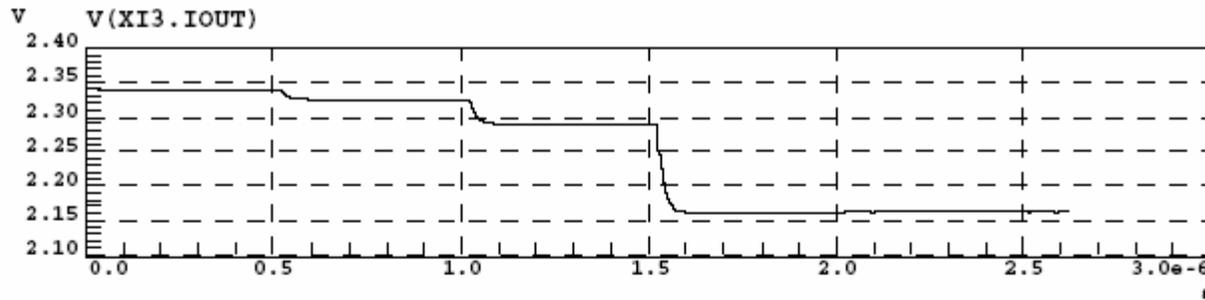
Read amplifier

*Input is the difference 0 – 2,
1 – 3; 2 – 4 etc.*

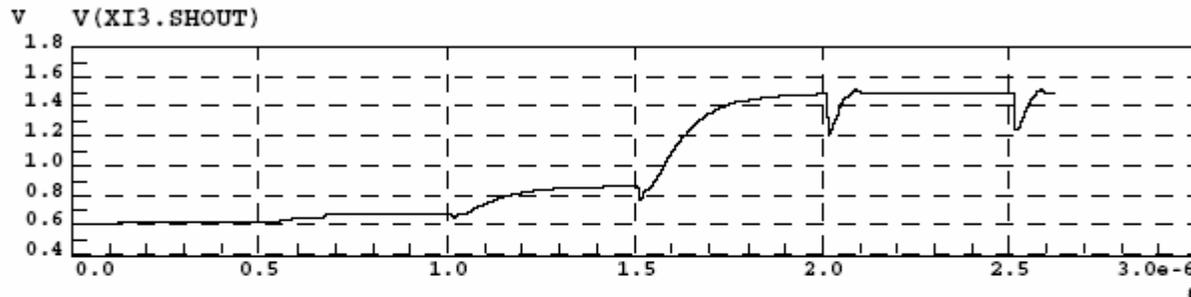


Ramp

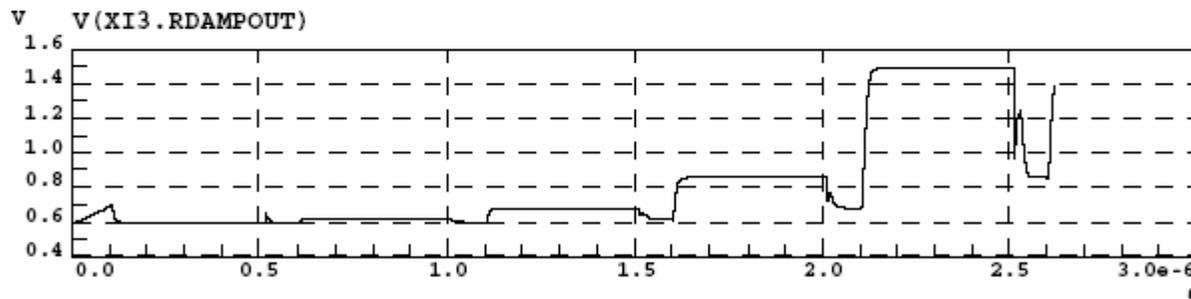
Simulations – Non-linear ramp



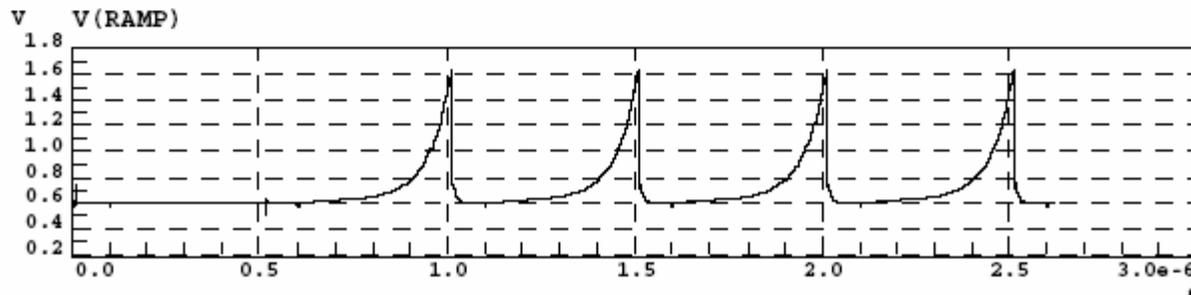
Integrator



Shaper



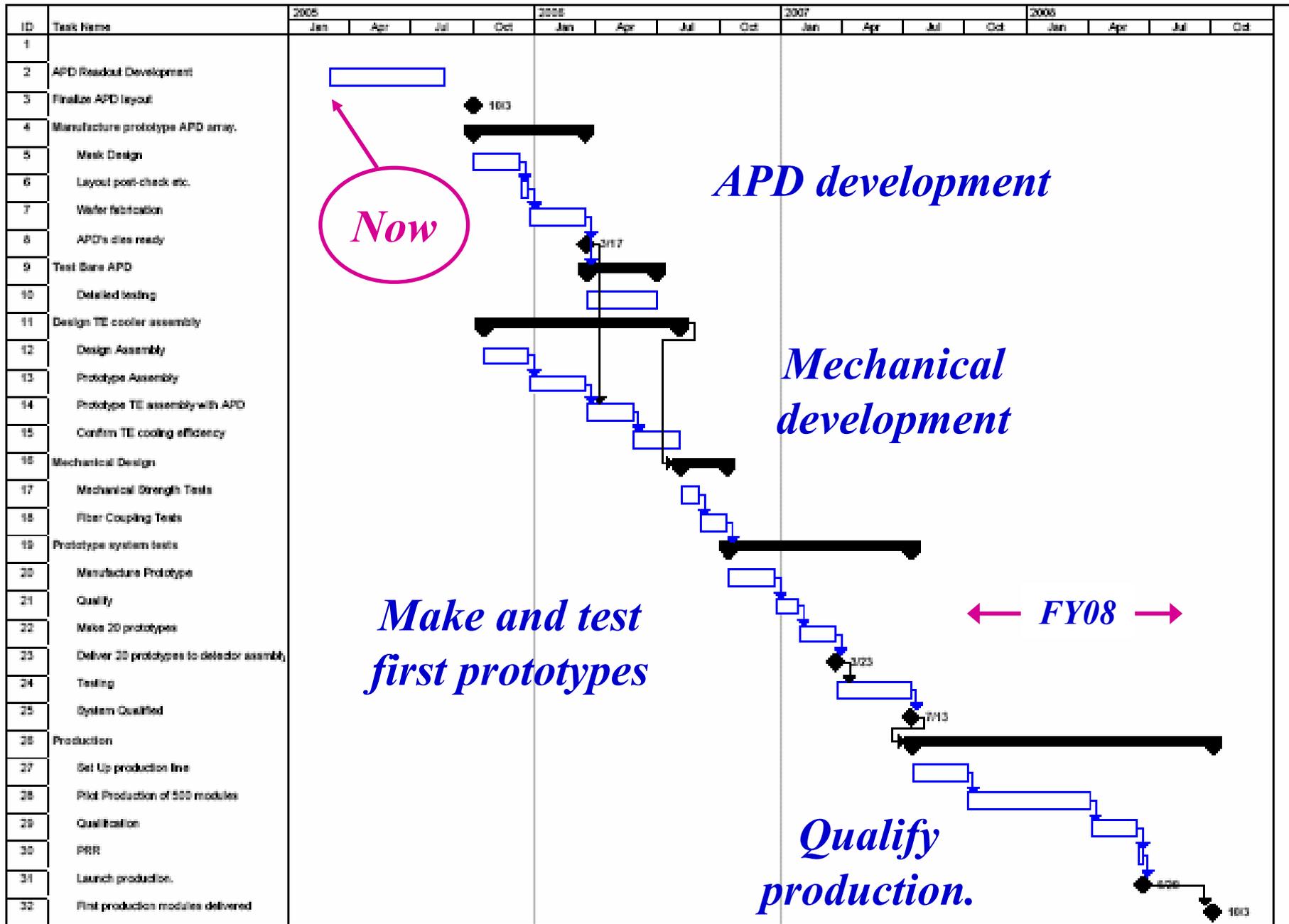
*Read
amplifier.*



Ramp

Development Schedule

- ◆ *Schedule to go from initial design concepts to launch production of 30,000 APD modules.*
- ◆ *There are four main steps to be done*
 - Design, make and qualify APD design.
 - Design make and qualify cooling system.
 - Prototype and test APD modules.
 - Qualify APD module production.
- ◆ *Each of these steps takes about 6 months.*
- ◆ *Some parallelism is possible, if resources are available.*
- ◆ *Simpler the manufacturing → fewer problems (normally).*



Summary

- ◆ *APD structure*
 - Some progress with APD design. Optimized for 32 channel modularity.
- ◆ *ASIC design of one version complete. Designed to meet beam and SN detector requirements.*
- ◆ *Schedule*
 - We need to start APD module design and development next year to be in full production by FY08.