

NOvA FEB

Programming Manual

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FEB Overview

The FEB utilizes registers in a 16 bit address and data space to control its functionality. One of these registers is used as a command register and the rest are used to specify details of how the FEB operates. This document describes the use of each register and is intended to be a programmer's users guide.

The details on the underlying communication protocol between the FEB and DCM are found in NOvA Document 814. This document includes the data packet structure and details on reading and writing FEB registers.

Control and Commands

Command Register

Commands are written to this register to control the operation of the FEB. The command is executed immediately following the write operation. The FEB will respond to the following commands.

Get Temperature 0x0020

Fetch the current temperature and put the result in the Temperature Register. This command is automatically issued internally every ~30s.

Serial Number Address Reset 0x0030

Reset the serial number character pointer to point to the first character in the string.

Reset FEB 0x1000

Put the FEB in a post configured state. This command will stop the DAQ, clear all memory and registers, restart the clock PLL, and reset communication with the DCM. It is intended that this command only be used during testing.

Start DAQ 0x1001

The Start DAQ command will enable the FEB to process and send data to the DCM. The method used to process data is set using the Mode Register.

Stop DAQ 0x1002

Immediately stop the current operation, stop sending data packets to the DCM, flush all data buffers and remain idle. The FEB will complete any data packet that has been started. The FEB will always maintain communication with the DCM and send the required status packets.

Start Time 0x2001

Start incrementing the FEB's current time.

Start Time 0x2002

Stop incrementing the FEB's current time.

Set NOvA APD Readout ASIC 0x3000

Program the APD Readout ASIC with the values that are contained in the ASIC programming Register.Global

Timing System Compatibility Registers

The registers in the range from 0x0000 to 0x00FF have been included to conform to the timing system address space and implementation on the DCM and TDU.

Timing Control Register

Bit 0 – Unused on FEB

Bit 1 – Enable FEB Current Time

This is equivalent to the Start Time Command.

Bit 2 – DCM Sync Enable

Enable the Sync signal to set the FEB current time to the Preset time. When disabled all sync signals will be ignored.

Bit 3 – Verify Enable.

Bit 4 – Unused on FEB

Bit 5 – Enable Status Frame

This bit enables the generation of the Status Frame to be sent.

Preset Time and Current Time Registers

The FEB internal current time is used to timestamp the APD data. The Preset Time Register is used in conjunction with the Sync signal on the FEB-DCM link to synchronize the current time on different FEBs. When the FEB receives the Sync signal it will set the current time to the contents of the Preset Time Register. The current time can be started and stopped using the corresponding FEB commands. Alternatively, the Timing Control Register can be used to start and stop the current time. Only the 29 MSBs can be set. The Default state of the FEB current time is stopped.

Version, Status, and Errors

Status Register

This register will contain the current FEB status. The bits are defined as follows.

Bit 15 – IS_ERROR (previously '0')
logical OR reduce of error flag register

Bit (14:7) - 0

Bit 6 – DCM_SYNC_EN
Set by DAQ

Bit 5 – ENABLE_STATUS_PKT
Set by DAQ

Bit 4 – ENABLE_TIME
Set by DAQ

Bit 3 – EVENT_FIFO_EMPTY
Condition of the FIFO responsible for buffering the data and timing marker packets before they are sent to the DCM.

Bit 2 – EVENT_FIFO_FULL (previously APD Data Buffer Full)
Condition of the FIFO responsible for buffering the data and timing marker packets before they are sent to the DCM.

Bit 1 – TECC_ENABLE (previously APD Data Buffer Empty)
State of the TECC_ENABLE signal as seen by the TECC.

Bit 0 - ENABLE_DAQ
Set by DAQ

Error Flag Register

FEB error flags are sticky until the error flag register is read. The bits are defined as follows.

Bit (15:10) - 0

Bit 9 – RX_Error
Unknown command frame from DCM

Bit 8 – TX_Error
Buffered event data unexpected length during TX to DCM

Bit 7 – READ_REG_Error

Error reading register during TX to DCM

Bit 6 – THEAD_OVFLW_ERR

Event data and time marker timestamp and data, pointer buffer overflow

Bit 5 – TDATA_OVFLW_ERR

Event data buffering overflow

Bit 4 – EVENT_OVFLW_ERR

Event data and timemarker data packet buffer overflow

Bit 3 - DATA_DROP_ERR (Previously ADC Error)

Data trigger ignored because of insufficient memory to handle event

Bit 2 - TECC_ERR_SHDN (Previously Overflow Error)

TECC auto monitoring detected an error condition.

Bit 1 - ADC_ERROR - (Previously Packet Error)

FEB4 - as reported by ADC

FEB5 – ADC serial interface detected a synchronization error

Bit 0 – COMM_ERROR

Serial data from DCM required resynchronization

Firmware Version Register

16 bit firmware version.

FEB-DCM Link - Status Frame

The Status Frame is generated once every second and sent to the DCM. It is enabled using the Timing Control Register. The Status packet reflects the contents of the Status register and Error Flag register. This is a change from the previous version.

Status Byte(7:6) <= Status Register(15:0)

Status Byte(5:4) <= Error Flag Register(15:0)

Status Byte(3:0) <= 0

The unused bits in in the status frame will be mapped to TECC monitoring registers in the next version.

FEB-DCM Link - Timing Marker Frame Status Bits

The high priority status and error flags are reported in the FEB-DCM link Timing Marker Frame. Bits (7:4) reflect the status register. Bits(3:0) reflect the Error

Flag register. Status bits are a snapshot of the current state of the FEB. Error flags are sticky until the error register is read.

Bit 7 – IS_ERROR(previously '0')

logical OR reduce of error flag register

Bit 6 – EVENT_FIFO_FULL (previously APD Data Buffer Full)

Condition of the FIFO responsible for buffering the data and timing marker packets before they are sent to the DCM.

Bit 5 – TECC_ENABLE (previously APD Data Buffer Empty)

State of the TECC_ENABLE signal as seen by the TECC.

Bit 4 - ENABLE_DAQ

Set by DAQ

Bit 3 - DATA_DROP_ERR (Previously ADC Error)

Data trigger ignored because of insufficient memory to handle event

Bit 2 - TECC_ERR_SHDN (Previously Overflow Error)

TECC auto monitoring detected an error condition.

Bit 1 - ADC_ERROR - (Previously Packet Error)

FEB4 - as reported by ADC

FEB5 – ADC serial interface detected a synchronization error

Bit 0 - COMM_ERROR

Serial data from DCM required resynchronization

Temperature Register

The Temperature Register is updated using the 'Get Temperature' command. Temperature data is represented by a 14-bit, two's complement word with a LSB equal to 0.03125°C. This register is automatically updated every ~30s

Serial Number Register

The Serial number is stored as ASCII values in non volatile memory on the FEB. The memory contains 128 characters and the first 12 characters represent the FEB's serial number. The first 6 characters of the serial number is the PCB version and the last 5 is the unique board identifier. e.g. FEB4.0-00016. The entire character string can be read using the Serial Number Register. Each time this register is read, the FEB returns the registers current value to the DCM and fetches the next character from the memory. The memory address pointer can be reset to point to the first character by writing the “Serial Number Address Reset” command to the Command Register.

The first character is read by resetting the address pointer and issuing two read commands to the serial number address. The first read will return the current register contents, fetch the first character from memory and place it in the register. The second read will return the first character to the DCM and fetch the second character from memory and place it in the register. This operation will return two register read results to the DCM but the first one is discarded. Each subsequent read will report the next ASCII character. At the end of the string the character pointer will roll over to the beginning.

Data Processing and Readout

Triggering and Sparsification

DAQ Mode Register

DCS DSP Mode 0x0000

This will be the normal running mode of the FEB. The FEB will digitize APD data from the Readout ASIC and process the incoming samples the FIR filtering coefficients (1 0 0 -1). If the filtered data exceeds its specified threshold value the channel is triggered. The trigger hold-off should be used to prevent subsequent triggers for a single event. The format of the resulting data packet is specified in NOVA Document 814.

Oscilloscope Mode 0x1000

The FEB will operate similar to a digital storage oscilloscope. The digitized APD data from the enabled channels will be buffered in one continuous time slice. Since the buffer memory is fixed and shared between all channels the length of the time slice is determined by the number of channels that are enabled. Oscilloscope mode is used in conjunction with the FEB's pulser functionality. When the FEB is enabled and ready to take data, the data buffer must be 'triggered' using the internal pulser signal. If the Event buffer becomes full, it will signal the FEB to stop taking data and put itself in idle mode. The number of contiguous samples returned is determined by the throughput, data buffer depth, and number of channels that are enabled. The Data Packet Regulator can be used to limit the amount of data returned while in Oscilloscope mode.

Memory Mode 0x2000 (not enabled in current version)

The FEBs output buffer is written to directly by the DCM.

Memory Loop Mode 0x2001(not enabled in current version)

The FEB's output buffer is written to directly by the DCM and it continuously loops.

Single Data Point Mode 0x3000(not enabled in current version)

In this mode the FEB will send a single data packet for every internal pulse it receives. This also enables Data packets to be sent at a selectable periodic rate. The packet sent is a single channel data point taken from the digitized APD data-stream.

Channel Enable Upper/Lower Register

Specify what channel data will end up in the output buffer. Bit number corresponds to channel number. Set to one enables channel. This bit is used the Normal DSP and Oscilloscope DAQ mode. During other test modes this register is ignored.

Trigger Threshold Registers

32 Trigger registers correspond to channel number

Data Packet Regulator Register

This 4 bit register regulates the number of contiguous data points that are returned when in DSO mode. The valid range of this register is 0 – 15. When set to 1, a single point from each channel will be returned. When this register is set to 4, a total of 128 data packets will be returned. This mode will operate with the pulser in either single or periodic mode. When this register is set to 0 the Regulator is disabled and the number of samples is determined by the throughput, data buffer depth, and number of channels that are enabled.

External Trigger Input

The FEB is capable of being triggered by an external source. The trigger input accepts a LVDS signal and uses a fixed data delay to allow latency on the trigger. Since this functionality is rarely used, the option must be selected before the firmware is synthesized and can be generated from the current version as needed.

Multipoint Readout

The Multipoint readout format will allow the number of data words and the data compression format to be specified by the DAQ. The following registers were added to control the Multipoint Readout process.

MP NSAMPLES Register

Specify the number of 16 bit data words in a data packet The DCM will accept only an even number of words.

DATA_PKT_ENCODE Register

Select the encoding format for data. This register controls both the type of data contained in the data packet and the position, relative to the trigger, of the first data point

DCS_N0 0x0

12 bit DCS value for each 16 bit word. First sample is first DCS value over threshold.

RAW_N1 0x1

12 bit ADC value for each 16 bit word. First sample starts at trigger time - 1

RAW_N2 0x2

12 bit ADC value for each 16 bit word. First sample starts at trigger time - 2

DATA_PKT_DAQID Register

The number of words in a data packet and encoding type will be assigned an arbitrary 5 bit tag that is set by the DAQ. This tag will appear in the data packet header bits (9:5) and allow the DAQ to decode and properly interpret the data contained in the packet.

Trigger Hold-off

The previous versions of firmware used a data packet that reported a single data point for each event, it was important for the trigger algorithm to find the maximum value over threshold. However, the Multipoint data will be aligned to the first event over threshold and produce a trigger for every event over threshold. A trigger that uses DCS coefficients [1 0 0 -1] will produce 3 consecutive triggers for a step input. The Multipoint Readout would result in 3 data packets with overlapping sample sequences. The Trigger hold-off can be used to mask the subsequent triggers and generate one data packet aligned with respect to the first event over threshold.

TRIG_HOLDOFF_TIME Register

Number of samples to mask a trigger after an initial trigger. FEB5 has a sample period of 125ns and FEB4 has a period of 500ns.

Legacy Mode

The FEB will default to Legacy mode where it will use the Multipoint readout architecture to emulate the data packet structure used in previous versions. This includes sending one data point followed by the constant 0xCAFE. The data point will be the ADC sample value when in oscilloscope mode and first DCS over threshold when in DAQ mode. The DAQ mode varies from the previous versions in that the previous version would use maximum DCS value over threshold. This can be changed if necessary. The FEB will use Legacy mode when MP SAMPLES is set to 0x00. DATA_PKT_DAQID should also be set to meet the requirements of the DAQ. All of the Multipoint Readout registers use the appropriate initial values which allows a FEB with new firmware to be compatible with the existing DAQ with no changes required .

ASIC Settings

ASIC Programming Registers

A description of the register settings can be found in NOVA Document 4371. Writing to these registers only sets the registers internal to the FPGA. The user must issue the command to program the ASIC with the values that have been set.

FEB-DCM Link - Timing Marker Frame

Timing Marker Packet Rate Register

The Timing Marker Packet Rate sets the rate Timing Marker Packets are sent to the DCM. The range is 0 – 255. 1 LSB = 1us. 00 = no timing markers and a power-up default is FF. Timing markers will bound the corresponding data packets and requires that the data packets be time sorted around the timing markers. Within the time markers the packets will generally be time ordered but this is not guaranteed. The timing markers will be sent only when time is enabled.

TECC Control and Monitoring

TECC Control

TECC Commands

These commands are written to the same FEB Command Register but they are used to interface with the TECC

Disable TECC 0x5000

The FEB powers up with the TECC disabled.

Enable TECC 0x5001

Get Drive Monitor 0x5020

Digitize the TECC Drive Monitor signal and store the results in the Drive Monitor Register. This command is automatically issued internally every ~30s.

Get Temp Monitor 0x5030

Digitize the TECC Temp Monitor signal and store the results in the Temp Monitor Register. This command is automatically issued internally every ~30s.

TECC Setpoint Register

12 bit ADC TECC setpoint adjustment.

TECC Drive Monitor Register

12 bit DAC drive monitor result. The contents of this register must be updated with the 'Get Drive Monitor' command sent to the command register. This register is automatically updated every ~30s.

TECC Temp Monitor Register

12 bit DAC drive monitor result. The contents of this register must be updated with the 'Get Temp Monitor' command sent to the command register. This register is automatically updated every ~30s.

TECC Auto Monitor and TECC Shutdown

Every ~30 sec the FEB will automatically digitize the value of the TECC Drive Monitor and Temp Monitor signals. The 12-bit ADC has a range of 0 to 2.048V. The FEB will flag an error condition if

(Temp Monitor > 0.35V) or (Drive Monitor > 1.95V, for a long time)

A long time is defined as the value of the TEC_DRIVE_ERR_THRSHLD register + 1 in minutes.

If an error is detected, the FEB will mask the TECC Enable signal. The error can only be cleared by a command from the DAQ to disable the TECC. This error will appear in the Error Flag register, Status packet and Timing packet.

TEC_DRIVE_ERR_THRSHLD Register

Used by the TECC Auto Monitor and Shutdown as a timeout on the TECC Drive signal to detect an over-drive error condition. The Timeout is the value of the register + 1 in minutes.

Pulse Generator and Trigger Output

Pulser Enable Register

The Pulser functionality is only used during debug and testing and can be left as disabled during normal operation. The FEB Pulser provides a way to synchronize the digitization of APD data with external APD light injection or charge injection into the Readout ASIC. This synchronization is required to catch the data that corresponds with an external stimulus. The Pulser Enable bits determine what part of the FEB will see the pulse. A common test performed is to start the FEB in oscilloscope mode and begin to record the digitized data. The external pulse is then used to trigger a calibrated injection of charge. The digitized data is then read out and analyzed. The scope of the pulser is selected using the following bits.

Bit 0 - Internal Pulse

Triggers the output buffer to collect a new set of data. This signal is pulsed in advance of the others to provide data before signals are injected.

Bit 1 - ASIC Testinject

Inject charge into unmasked channels via the ASIC's internal charge injection circuit. The amount of charge and channel mask are set using the ASIC Programming registers. This method of charge injection is not intended as a calibration method.

Bit 2 - External Pulse

Enables the external pulse output that can be used with instruments such as oscilloscopes and pulse generators.

Pulser Periodicity Register

The pulse can be a single shot or periodic. When Pulser Periodicity is set to "0x0001", the write process will cause a single pulse event. Otherwise a pulse will periodically be sent with a period of $1\mu\text{s} * \text{Pulser Periodicity}$.

External Pulser Width Register

Sets the pulse width of the External pulse.

High Voltage Adjustment

The APD high voltage is set via a shunt regulator on the FEB and controlled using this register. The register is 12 bits and the voltage follows the following function.

$\text{Voltage} = 0.0257 * \text{Reg} + 299.$

The FEB will power up with the voltage at its maximum setting.

Register Address Map

Global Timing System Registers			
0x0000	Timing Control		
0x0010	Preset_Time_L(15:2)	R/W	0x0000
0x0011	Preset_Time_U(15:0)	R/W	0x0000
0x0012	reserved		
0x0013	reserved		
FEB command and Status			
0x0101	Command(15:0)	W	
0x0102	Status(15:0)	R	
0x0103	Error Flag(15:0)	R	
0x0104	Firmware_version	R	
0x0120	Temperature(13:0)	R	0x000
0x0121	Temperature_Timestamp_L(15:0)	R	0x0000
0x0122	Temperature_Timestamp_U(15:0)	R	0x0000
0x0030	Serial Number(15:0)	R	
Registers to control the FEB modes of operation			
0x1000	DAQ Mode(15:0)	R/W	0x0000
0x1001	Channel Enable Upper(15:0)	R/W	0xFFFF
0x1002	Channel Enable Lower(15:0)	R/W	0xFFFF
0x1010	Timing Marker Packet Rate	R/W	0xFF
0x1020	High Voltage Adjust	R/W	0xFFF
0x1030	DATA REGULATOR	R/W	0X0
0x1040	MP_NSAMPLES(4:0)	R/W	0X00
0x1041	DATA_PKT_ENCODE(3:0)	R/W	0X1
0x1042	DATA_PKT_DAQID(4:0)	R/W	0X00
0x1050	TRIG_HOLDOFF_TIME(3:0)	R/W	0X8
Trigger threshold			
0x2000	Trigger threshold Ch0(12:0)	R/W	0x000
0x2001	Trigger threshold Ch1(12:0)	R/W	0x000
...	...		
0x201F	Trigger threshold Ch31(12:0)	R/W	0x000
TECC Status and Control			
0x5010	Setpoint(11:0)	R/W	0x000

0x5020	Drive Monitor(11:0)	R	0x000
0x5021	Drive Monitor_Timestamp_L(15:0)	R	0x0000
0x5022	Drive Monitor_Timestamp_U(15:0)	R	0x0000
0x5023	TEC_DRIVE_ERR_THRSHLD(2:0)	R/W	0x0
0x5030	Temp Monitor(11:0)	R	0x000
0x5031	Temp Monitor_Timestamp_L(15:0)	R	0x0000
0x5032	Temp Monitor_Timestamp_U(15:0)	R	0x0000
0x5032	Drive Timeout Threshold(11:0)	R/W	0xFFFF
0x5032	Drive Timeout Length(15:0)	R/W	0xFFFF
ASIC Programming Registers			
0x4040	Spare(0:5)	R/W	
0x4041	VtSel(0:2)	R/W	
0x4042	RefSel(0:3)	R/W	
0x4043	ISel(0:2)	R/W	
0x4044	BWsel(0:3)	R/W	
0x4045	GSel(0:2)	R/W	
0x4046	TfSel(0:2)	R/W	
0x4047	Mux2to1(0)	R/W	
0x4048	Mux8to1(0)	R/W	
0x4000	Offs0(0:4) (channel 0)	R/W	
0x4020	Mask0 (0) (channel 0)	R/W	
0x4001	Offs1(0:4) (channel 1)	R/W	
0x4021	Mask1(0) (channel 1)	R/W	
0x4002	Offs1(0:4) (channel 2)	R/W	
0x4022	Mask1(0) (channel 2)	R/W	
...	...		
...	...		
0x401f	Offs31(0:4) (channel 31)	R/W	
0x403f	Mask31 (channel 31)	R/W	
DSP Filter coefficients			
0x8xxx	TBD	R/W	
0x9xxx	TBD	R/W	
0xAxxx	TBD	R/W	
Registers only used during testing and debugging			
0xF000	Pulser Enable(15:0)	R/W	0x0000
0xF001	Pulser Periodicity(15:0)	R/W	0x0000
0xF002	Pulser Width(15:0)	R/W	0x0000
0xF020	sel_seg(15:0)	R/W	0x0000
Reserved Addresses 0xe000 - 0xEFFF			
0xE005	DCM Emulator internal		

Known Issues and To Do list

Status Reporting

Put TECC Monitor auto update results in Status Register

Memory Modes

The Memory test modes are not implemented.

Single Data Point Mode

Put this back.

Multipoint Readout

Implement floating point data format option

Trigger

Implement matched filter trigger option

ASIC Offsets

Implement a command to auto adjust the ASIC offset values.

Documentation

Documentation of DCM Emulator, USB readout, MiniDAQ, and custom drivers.

Sync Signal Handling (still needed?)

Set the preset time and imitate with sinc signal. The Sinc signal should only preset the time when following a preset register write.

Send Sinc acknowledge in the form of a status packet.

Firmware Revisions

FebV4.00.01	2010, July 23	Read and Write registers. Oscilloscope mode is the only mode operational.
FebV4.00.02	2010, August 10	Changes to Logic Analyzer Port Signals
FebV4.00.03	2010, August 16	Changes to Logic Analyzer Port Signals
FebV4.00.04	2010, August 24	Added Firmware Version Register , Status Register and Error Register
FebV4.00.05	2010, August 24	Every DAQ mode will result in a Single Data Point Mode. Timing Packet markers are now being sent at ~8us
FebV4.00.06	2010, August 25	Timing marker rate is set to 500ms to try to help debugging.
FebV4.00.07	2010, August 26	The DCS mode, Oscilloscope mode, and Single Data Point mode are functioning as described in this document. The DAQ mode must be set correctly. In previous versions only one mode was functional per version.
FebV4.00.08	2010, August 28	Register 1010 selects Timing Marker Packet rate with 1 LSB = 4us , 0000 = off and powerup default = ffff
FebV4.00.0E	2010, October1	Changed Current time to allow for synchronization between time markers across multiple boards
FebV4.00.0F	2010, Oct 12	Added the Data Regulator
FebV4.00.10	2010, Oct 20	Enabled the Channel enable bits for DCS and Oscope modes. Internally inverted the HV setting bits so that 000 is the low setting and FFF is the high setting.
FebV4.00.12	2010,Nov 5	Global timing compatibility, Status Frame,Status in timing markers, Synchronization using Sync signal.
FebV4.00.13	2011 Jun 20	Data packet timestamps will now be contained within its corresponding timemarkers. The LSB of the Time_Marker_Rate register is 1us
FebV4.00.15	2011 Jul 05	Vertical Slice version which delays Data by 5us and adds external trigger input.
FebV4.00.16		HV Register read back is correct
FebV4.1.0030	2012 May 18	Fixed channel enable mapping problem. Software tools update and recompile

FebV4.10.20	2013 Sep 11	
FebV4.10.22	2013 Jan 16	Implements the “multi-point” readout where the number of data words included in a data packet is settable. This version should be only be considered for multipoint data packet testing as some functions are temporary disabled. For more information on this version please see Release Notes for Firmware Version FebV4.10.22.
FebV4.10.23	2013 Jun 17	<p>This version introduces Legacy mode as a default configuration.</p> <p>TECC automatic monitoring and shutdown is introduced in this version.</p> <p>Error and Status bits have been remapped to make high priority events more visible</p> <p>Oscope and DCS DSP mode are operational in both Legacy and Multipoint data packet packet formats. Single data point mode is not functional.</p> <p>Includes the trigger holdoff feature to limit the number of data packets per trigger.</p> <p>Includes the DATA_PKT_DAQID register to specify the 5 bit data type tag in the data packet header.</p> <p>Trigger head memory increased to allow for less efficient Legacy mode data format.</p> <p>Uses a unified version of firmware that is shared with FEB V5</p>
FebV4.10.24	2013 Jun 24	<p>Fixed FEB sync problem where timestamps of time marker packets between multiple FEBs could be 1us out of sinc after the initial sync pulse.</p> <p>All functionality as in version FebV4.10.23.</p>

