

# NOvA FEB

## Programming Manual

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Nathan Felt, John Oliver

Harvard University

Laboratory for Particle Physics and Cosmology

Detector Electronics Facility

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## FEB Overview

The FEB utilizes registers in a 16 bit address and data space to control its functionality. One of these registers is used as a command register and the rest are used to specify details of how the FEB operates. This document describes the use of each register and is intended to be a programmer's users guide.

The details on the underlying communication protocol between the FEB and DCM are found in NOVA Document 814. This document includes the data packet structure and details on reading and writing FEB registers.

## FEB Register Definitions

### Command

Commands are written to this register to control the operation of the FEB. The command is executed immediately following the write operation. The FEB will respond to the following commands.

#### Get Temperature 0x0020

Fetch the current temperature and put the result in the Temperature Register.

#### Serial Number Address Reset 0x0030

Reset the serial number character pointer to point to the first character in the string.

#### Reset FEB 0x1000

Put the FEB in a post configured state. This command will stop the DAQ, clear all memory and registers, restart the clock PLL, and reset communication with the DCM. It is intended that this command only be used during testing.

#### Start DAQ 0x1001

The Start DAQ command will enable the FEB to process and send data to the DCM. The method used to process data is set using the Mode Register.

#### Stop DAQ 0x1002

Immediately stop the current operation, stop sending data packets to the DCM, flush all data buffers and remain idle. The FEB will complete any data packet

that has been started. The FEB will always maintain communication with the DCM and send the required status packets.

#### Start Time 0x2001

Start incrementing the FEB's current time.

#### Start Time 0x2002

Stop incrementing the FEB's current time.

#### Set NOvA APD Readout ASIC 0x3000

Program the APD Readout ASIC with the values that are contained in the ASIC programming Register.

### TECC Commands

These commands are written to the same FEB Command Register but they are used to interface with the TECC

#### Disable TECC 0x5000

The FEB powers up with the TECC disabled.

#### Enable TECC 0x5001

#### Get Drive Monitor 0x5020

Digitize the TECC Drive Monitor signal and store the results in the Drive Monitor Register.

#### Get Temp Monitor 0x5030

Digitize the TECC Temp Monitor signal and store the results in the Temp Monitor Register.

### Status

This register will contain the instantaneous FEB status. The bits are defined as follows.

#### Bit 0 – Enable DAQ

'1' if FEB is currently enabled and taking data

Bit 1 – APD Data Buffer Empty

Bit 2 – APD Data Buffer Full

## Error Flag

When an error is detected it will be flagged by setting a bit in the Error Flag. When this register is read it will automatically clear all error bits. The definition of the bits is as follows.

Bit 0 – Communication Error

A communication error will occur when a 8b10b protocol error has been detected on the DCM Link Command signal.

Bit 1 – Packet Error

A Packet Error will occur when a DCM command packet is not recognized as a valid packet.

Bit 2 – Overflow Error

Data has been lost due to a full APD data buffer

Bit 3 – ADC Error

The FEB's APD data quad ADC is reporting an internal error.

## Firmware Version

16 bit hex firmware version.

## Temperature

The Temperature Register is updated using the 'Get Temperature' command. Temperature data is represented by a 14-bit, two's complement word with a LSB equal to 0.03125°C

## Serial Number Register

The Serial number is stored as ASCII values in non volatile memory on the FEB. The memory contains 128 characters and the first 12 characters represent the FEB's serial number. The first 6 characters of the serial number is the PCB version and the last 5 is the unique board identifier. e.g. FEB4.0-00016. The

entire character string can be read using the Serial Number Register. Each time this register is read, the FEB returns the registers current value to the DCM and fetches the next character from the memory. The memory address pointer can be reset to point to the first character by writing the “Serial Number Address Reset” command to the Command Register.

The first character is read by resetting the address pointer and issuing two read commands to the serial number address. The first read will return the current register contents, fetch the first character from memory and place it in the register. The second read will return the first character to the DCM and fetch the second character from memory and place it in the register. This operation will return two register read results to the DCM but the first one is discarded. Each subsequent read will report the next ASCII character. At the end of the string the character pointer will roll over to the beginning.

## DAQ Mode

### DCS DSP Mode 0x0000

This will be the normal running mode of the FEB. The FEB will digitize APD data from the Readout ASIC and process the incoming samples the FIR filtering coefficients (1 0 0 -1). If the filtered data exceeds its specified threshold value the channel is marked as being triggered. A channel is in this triggered state until the DCS value falls below 0 the threshold value when it then enters a readout state. During the readout state it will wait to be put into the readout buffer. The readout buffer can only be written to by one channel at a time, therefore, if multiple channels enter a readout state simultaneously each channel will need to wait for its turn to be put into the buffer. The format of the resulting data packet is specified in NOVA Document 814.

### Oscilloscope mode 0x1000

The FEB will operate similar to a digital storage oscilloscope. The digitized APD data from the enabled channels will be buffered in one continuous time slice. Since the buffer memory is fixed and shared between all channels the length of the time slice is determined by the number of channels that are enabled. Each sample will be sent one data packet at a time using the same format as normal DSP mode.

Oscilloscope mode is used in conjunction with the FEB's pulser functionality. When the FEB is enabled and ready to take data, the data buffer must be 'triggered' using the internal pulser signal. The data buffer will record data samples until it is full.

## Memory Mode 0x2000

The FEBs output buffer is written to directly by the DCM.

## Memory Loop Mode 0x2001

The FEB's output buffer is written to directly by the DCM and it continuously loops.

## Single Data Point Mode 0x3000

In this mode the FEB will send a single data packet for every internal pulse it receives. This also enables Data packets to be sent at a selectable periodic rate. The packet sent is a single channel data point taken from the digitized APD data-stream.

## Channel Enable Upper/Lower

Specify what channel data will end up in the output buffer. Bit number corresponds to channel number. Set to one enables channel. This bit is used the Normal DSP and Oscilloscope DAQ mode. During other test modes this register is ignored.

## Timing Marker Packet Rate

Sets the rate a Timing Marker Packet is sent to the DCM. The range is 0 – 255. 1 LSB = 1us. 00 = no timing markers and a power-up default is FF. Timing markers have priority over the the data packets. If lots of data is queued, eg Oscope mode, the Data packets will fill in the gaps between timing markers. Since the timing markers have priority, the presence of data doesn't change the periodic rate of the timing markers. The timing markers will be sent only when time is enabled.

## High Voltage Adjustment

The APD high voltage is set via a shunt regulator on the FEB and controlled using this register. The register is 12 bits and the voltage follows the following function.

$$\text{Voltage} = 0.0257 * \text{Reg} + 299.$$

The FEB will power up with the voltage at its maximum setting.

## Data Packet Regulator

This 4 bit register regulates the number of contiguous data points that are returned when in DSO mode. The valid range of this register is 0 – 15. When set to 1, a single point from each channel will be returned. When this register is set to 4, a total of 128 data packets will be returned. This mode will operate with the pulser in either single or periodic mode. When this register is set to 0 the Regulator is disabled and the number of samples is determined by the throughput and data buffer depth.

## TECC Setpoint

12 bit ADC TECC setpoint adjustment.

## TECC Drive Monitor

12 bit DAC drive monitor result. The contents of this register must be updated with the 'Get Drive Monitor' command sent to the command register.

## TECC Temp Monitor

12 bit DAC drive monitor result. The contents of this register must be updated with the 'Get Temp Monitor' command sent to the command register.

## Trigger threshold

32 Trigger registers correspond to channel number

## ASIC Programming Register

A description of the register settings can be found in NOVA Document 4371. Writing to these registers only sets the registers internal to the FPGA. The user must issue the command to program the ASIC with the values that have been set.

## Pulser Enable

The Pulser functionality is only used during debug and testing and can be left as disabled during normal operation. The FEB Pulser provides a way to synchronize the digitization of APD data with external APD light injection or charge injection into the Readout ASIC. This synchronization is required to catch the data that corresponds with an external stimulus. The Pulser Enable bits determine what part of the FEB will see the pulse. A common test performed is to start the FEB in oscilloscope mode and begin to record the digitized data. The external pulse is

then used to trigger a calibrated injection of charge. The digitized data is then read out and analyzed. The scope of the pulser is selected using the following bits.

### Internal Pulse Bit 0

Triggers the output buffer to collect a new set of data. This signal is pulsed in advance of the others to provide data before signals are injected.

### ASIC Testinject Bit 2

Inject charge into unmasked channels via the ASIC's internal charge injection circuit. The amount of charge and channel mask are set using the ASIC Programming registers. This method of charge injection is not intended as a calibration method.

### External Pulse Bit 2

Enables the external pulse output that can be used with instruments such as oscilloscopes and pulse generators .

## Pulser Periodicity

The pulse can be a single shot or periodic. When Pulser Periodicity is set to "0x0001", the write process will cause a single pulse event. Otherwise a pulse will periodically be sent with a period of  $1\mu\text{s} * \text{Pulser Periodicity}$ .

## External Pulser Width

Sets the pulse width of the External pulse.

## Global Timing System Compatibility Registers

The registers in the range from 0x0000 to 0x00FF have been included to conform to the timing system address space and implementation on the DCM and TDU.

## Timing Control

Bit 0 – Unused on FEB

Bit 1 – Enable FEB Current Time

This is equivalent to the Start Time Command.

### Bit 2 – Preset Enable

Enable the Sync signal to set the FEB current time to the Preset time. When disabled all sync signals will be ignored.

### Bit 3 –Verify Enable.

### Bit 4 – Unused on FEB.

### Bit 5 – Enable Status Frame

This bit enables the generation of the Status Frame to be sent.

## Preset Time and Current Time

The FEB internal current time is used to timestamp the APD data. The Preset Time Register is used in conjunction with the Sync signal on the FEB-DCM link to synchronize the current time on different FEBs. When the FEB receives the Sync signal it will set the current time to the contents of the Preset Time Register. The current time can be started and stopped using the corresponding FEB commands. Alternatively, the Timing Control Register can be used to start and stop the current time. Only the 29 MSBs can be set. The Default state of the FEB current time is stopped.

## FEB-DCM Link Frames

### Status Frame

The Status Frame is sent periodically via the FEB-DCM link once every second. It is enabled using the Timing Control Register. The status packet currently has 7 bits defined and 57 bits set to a constant value. The information reported in the. Is defined as follows.

byte 7

bit 7 '0'

bit 6 FEB\_BUFFER\_FULL

bit 5 FEB\_BUFFER\_EMPTY

bit 4 ENABLE\_DAQ (ie Process new data)

bit 3 ADC\_ERROR (As reported by CERN quad ADC)

bit 2 Overflow Error

bit 1 Packet Error

bit 0 Comm Error

byte 6 - byte 0

Constant "0x0000000CAB005E"

Currently the bits that reflect errors are not latched as they are in the FEBs Error Register. This will be changed in the next version such that the error bits (bits 0 – 3 ) will be latched until the packet is transmitted. When an error occurs briefly between status packets, it will be guaranteed to be sent once and the time interval the error occurred is known. The status bits (bits 4 – 7 ) reflect the current state of the FEB and will not be latched.

Also, more status bits will be defined later versions such as TECC monitoring.

## Timing Marker Frame FEB Status

The FEB status reported in the DCM – FEB link Timing Marker Frame. Is defined as follows

bit 7 '0'

bit 6 FEB\_BUFFER\_FULL

bit 5 FEB\_BUFFER\_EMPTY

bit 4 ENABLE\_DAQ (ie Process new data)

bit 3 ADC\_ERROR (As reported by CERN quad ADC)

bit 2 Overflow Error

bit 1 Packet Error

bit 0 Comm Error

Currently, the bits that reflect errors (bits 0 – 3 ) are not latched as they are in the FEBs error Register. This will be changed in the next version such that the error bits will be latched until the packet is transmitted. When an error occurs briefly between timing markers, it will be guaranteed to be sent once and the time interval the error occurred is known. The status bits (bits 4 – 7 ) reflect the current state of the FEB and will not be latched.

Address	Contents (Valid:Bits)	Direction	Default Value
<b>Global Timing System Registers</b>			
0x0000	Timing Control		
0x0010	Preset_Time_L(15:2)	R/W	0x0000
0x0011	Preset_Time_U(15:0)	R/W	0x0000
0x0012	reserved		
0x0013	reserved		
<b>FEB command and Status</b>			
0x0101	Command(15:0)	W	
0x0102	Status(15:0)	R	
0x0103	Error Flag(15:0)	R	
0x0104	Firmware_version	R	
0x0120	Temperature(13:0)	R	0x000
0x0121	Temperature_Timestamp_L(15:0)	R	0x0000
0x0122	Temperature_Timestamp_U(15:0)	R	0x0000
<b>Registers to control the FEB modes of operation</b>			
0x1000	DAQ Mode(15:0)	R/W	0x0000
0x1001	Channel Enable Upper(15:0)	R/W	0xFFFF
0x1002	Channel Enable Lower(15:0)	R/W	0xFFFF
0x1010	Timing Marker Packet Rate	R/W	0xFF
0x1020	High Voltage Adjust	R/W	0xFFF
0x1030	DATA REGULATOR	R/W	0X0
<b>Trigger threshold</b>			
0x2000	Trigger threshold Ch0(12:0)	R/W	0x000
0x2001	Trigger threshold Ch1(12:0)	R/W	0x000
...	...		
0x201F	Trigger threshold Ch31(12:0)	R/W	0x000
<b>TECC Status and Control</b>			
0x5010	Setpoint(11:0)	R/W	0x000
0x5020	Drive Monitor(11:0)	R	0x000
0x5021	Drive Monitor_Timestamp_L(15:0)	R	0x0000
0x5022	Drive Monitor_Timestamp_U(15:0)	R	0x0000
0x5030	Temp Monitor(11:0)	R	0x000
0x5031	Temp Monitor_Timestamp_L(15:0)	R	0x0000
0x5032	Temp Monitor_Timestamp_U(15:0)	R	0x0000
<b>ASIC Programming Registers</b>			

0x4040	Spare(0:5)	R/W	
0x4041	VtSel(0:2)	R/W	
0x4042	RefSel(0:3)	R/W	
0x4043	ISel(0:2)	R/W	
0x4044	BWSEL(0:3)	R/W	
0x4045	GSel(0:2)	R/W	
0x4046	TfSel(0:2)	R/W	
0x4047	Mux2to1(0)	R/W	
0x4048	Mux8to1(0)	R/W	
0x4000	Offs0(0:4) (channel 0)	R/W	
0x4020	Mask0 (0) (channel 0)	R/W	
0x4001	Offs1(0:4) (channel 1)	R/W	
0x4021	Mask1(0) (channel 1)	R/W	
0x4002	Offs1(0:4) (channel 2)	R/W	
0x4022	Mask1(0) (channel 2)	R/W	
...	...		
...	...		
0x401f	Offs31(0:4) (channel 31)	R/W	
0x403f	Mask31 (channel 31)	R/W	
DSP Filter coefficients			
0x8xxx	TBD	R/W	
0x9xxx	TBD	R/W	
0xAxxx	TBD	R/W	
Registers only used during testing and debugging			
0xF000	Pulser Enable(15:0)	R/W	0x0000
0xF001	Pulser Periodicity(15:0)	R/W	0x0000
0xF002	Pulser Width(15:0)	R/W	0x0000
Reserved Addresses 0xe000 - 0xEFFF			
0xE005	DCM Emulator internal		

## Known Issues and To Do list

Let me know of any bugs or feature change/requests. And I'll put them in the queue.

### Time Markers

Currently it is not guaranteed that the data packet timestamps will be contained within its corresponding timemarkers and it also looks like the value of the LSB needs to be adjusted. This will be fixed soon.

### Status Packet

Currently, the bits that reflect errors (bits 0 – 3 ) are not latched as they are in the FEBs error Register. This will be changed in the next version such that the error bits will be latched until the packet is transmitted. When an error occurs briefly between timing markers, it will be guaranteed to be sent once and the time interval the error occurred is known. The status bits (bits 4 – 7 ) reflect the current state of the FEB and will not be latched.

### Memory Modes

The Memory test modes are not implemented.

### Start time command

The start time command will be redefined to start the FEB current time on the next sync rather than immediately.

### Global Timing System registers compatibility

There needs some clarification of the Global Timing System registers for compatibility. The operation of the FEB status frame is different then the DCM status frame as it is being sent periodically not requested by setting the report status bit. Also, the information included in the Status Frame not limited to the Global Timing System. This also impacts the function of the verify enable bit. The Timing System Interface Status Register is defined as 'reserved' in the DCM Users Guide.

### Current time clock

look into a potential clocking problem that will cause a FEBs current time to be skewed by 31 ns. The time markers will still be the same.

## ASIC Offsets

implement a command to auto adjust the ASIC offset values.

## Document Revisions

2010, August 17	Added Firmware Version Register
2010, August 25	Added the Single Data Point DAQ Mode are working as described in this document.
2010, August 26	Included the Firmware Revision Log
2010, August 31	Added HV register, Added Timing marker Packet adjustment register. Fixed the TECC status and control registers.
2010, October 20	Serial number, HV reg settings. TECC control commands and registers. Oscopce Data regulator. Defined Status and error bits. Added known Issues List
2010, Nov 17	Global timing compatibility, Status packet, Synchronization using Sync signal.

## Firmware Revisions

FebV4.00.01	2010, July 23	Read and Write registers. Oscilloscope mode is the only mode operational.
FebV4.00.02	2010, August 10	Changes to Logic Analyzer Port Signals
FebV4.00.03	2010, August 16	Changes to Logic Analyzer Port Signals
FebV4.00.04	2010, August 24	Added Firmware Version Register , Status Register and Error Register
FebV4.00.05	2010, August 24	Every DAQ mode will result in a Single Data Point Mode. Timing Packet markers are now being sent at ~8us
FebV4.00.06	2010, August 25	Timing marker rate is set to 500ms to try to help debugging.
FebV4.00.07	2010, August 26	The DCS mode, Oscilloscope mode, and Single Data Point mode are functioning as described in this document. The DAQ mode must be set correctly. In previous versions only one mode was functional per version.
FebV4.00.08	2010, August 28	Register 1010 selects Timing Marker Packet rate with 1 LSB = 4us , 0000 = off and powerup default = ffff
FebV4.00.0E	2010, October1	Changed Current time to allow for synchronization between time markers across multiple boards
FebV4.00.0F	2010, Oct 12	Added the Data Regulator
FebV4.00.10	2010, Oct 20	Enabled the Channel enable bits for DCS and Oscope modes. Internally inverted the HV setting bits so that 000 is the low setting and FFF is the high setting.
FebV4.00.12	2010,Nov 5	Global timing compatibility, Status Frame,Status in timing markers, Synchronization using Sync signal.