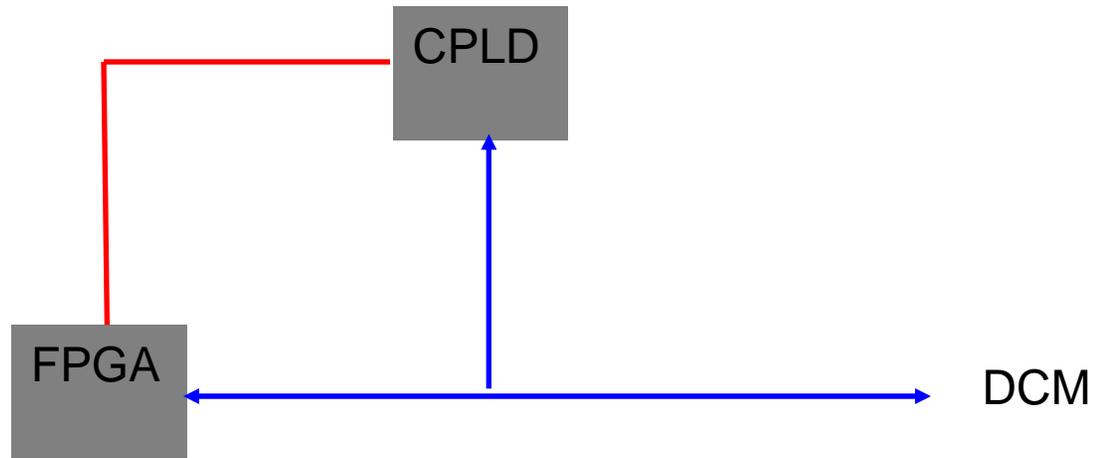


CPLD looks for sync to be held true or some pattern to indicate program mode.

Configuration data is sent on the command signal.



Programming is the same as before except the FPGA is Configured directly by the DCM which must be done at power up

Board cost savings.

Less likely that multiple boards will have different firmware