Link Interface Specification for the Nova Front End Board to Data Concentrator Module Connection (Draft)

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Introduction

This specification defines the cables, connectors, pinouts, electrical requirements, and communication protocol for the Nova Front-End Board (FEB) to Data Concentrator Module (DCM) data links. To reduce cost and simplify specification and acquisition of the data link cabling, Category 5 (CAT5) cables with RJ-45 plugs will be used. On the modules, mating RJ-45 jacks will be used. Data communication will be 8b-10b encoded, while clock and sync will be unencoded on separate wire pairs in the CAT5 cables.

Cables and Connectors

CAT5 cables with RJ-45 plugs are to be wired in a straight-through T568A or T568B configuration (Ref: ANSI/TIA/EIA-568.B). Plugs can be connected in either T568A or B configuration, but the same configuration must be used on both ends of the cable. Cables, plugs, and jacks meeting the ANSI/TIA/EIA-568.B series of specifications are acceptable. Note that since most cables of this type are used for 10/100 Ethernet, it may be possible to find cables with only two pairs of wires connected. For Nova, it is required that all four pairs of wires are connected as specified. CAT5e and CAT6 cables can also be used, but are generally more expensive due to their higher specified bandwidth.

CAT5 cables contain four twisted-pairs of wires with no shield. T568A termination of the four pairs of wires specifies that an RJ-45 plug is connected as shown in Figure 1. T568B termination of cables is similar, but the green and orange pairs are swapped with each other at the plug connection as shown in Figure 2. Either T568A termination or T568B termination can be used, but for each cable, plugs must use the same termination specification at *both ends of the cable*.

Pair	*Wire Pairs(pin number and color)*
1	4 (- blue) and 5 (+ white/blue)
2	3 (+ white/orange) and 6 (- orange)
3	1 (+ White/green) and 2 (- green)
4	7 (+white/brown) and 8 (- brown)

Figure 1 CAT5 Twisted Pairs as Wired in T568A Configuration

Pair	*Wire Pairs(pin number and color)*
1	4 (- blue) and 5 (+ white/blue)
2	1 (+ white/orange and 2 (- orange)
3	3 (+ White/green) and 6 (- green)
4	7 (+white/brown) and 8 (- brown)

Figure 2 CAT5 Twisted Pairs as Wired in T568B Configuration

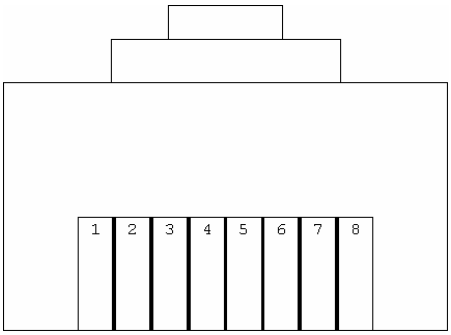

Figure 3 View Looking at Face of RJ-45 Plug

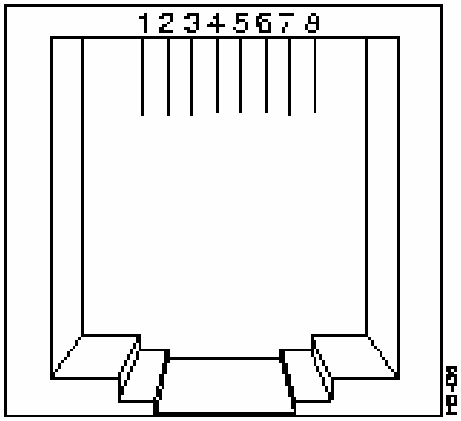

Figure 4 View Looking Into RJ-45 Jack

Pinout of RJ-45 Connector at Data Concentrator Module

The data link jack on the Data Concentrator Module is defined in Figure 5.

Pin	*Function*
1	Transmit Sync +
2	Transmit Sync –
3	Receive Data +
4	Transmit Clock -
5	Transmit Clock +
6	Receive Data -
7	Transmit Command +
8	Transmit Command -

Figure 5 Data Link Pinout at DCM

Pinout of RJ-45 Connector at Front End Board

The data link jack on the Front End Board is defined in Figure 6.

Pin	*Function*
1	Receive Sync +
2	Receive Sync -
3	Transmit Data +
4	Receive Clock -
5	Receive Clock +
6	Transmit Data -
7	Receive Command +
8	Receive Command -

Figure 6 Data Link Pinout at FEM

Electrical

Each of the four differential pairs on the data link is defined as conforming to the Low-Voltage Differential Signaling (LVDS) standard. No termination is required at the driver, but a 100 ohm differential termination is required at the receiver. 100 ohm differential impedance control should be enforced on all circuit board traces, connectors, and cables.

Since the FEBs and the DCM are reference grounded at the same point, and the voltage drop in the Front-End power cables is specified to be small (<100mV), AC coupling of the LVDS pairs is unnecessary. DC coupling simplifies the design of both the FEBs and the DCMs, since ensuring a DC balanced signal is not required.

Communication Protocol

For this discussion, each of the four wire pairs in the cable will be referred to as a channel. The four channels are: Data, Command, Clock, and Sync. Command, Clock, and Sync are driven by DCM and received by FEB. The Data channel is driven by FEB and received by DCM. The Data and Command channels use 8b-10b data encoding (Ref:

Widmer and Franaszek) to ensure robust data and command transmission. The Clock channel will run at the front-end clock frequency. The Sync channel is synchronous with the clock channel and is unencoded,. Sync is considered false when low and true when high. A logic high is defined as signal+ positive voltage relative to signal- for the differential LVDS signals. Sync level transitions will lead Clock level transitions by approximately 90 degrees. FEBs sample Sync as valid on the rising edge of Clock.

On the Data and Command channels, data is encoded in an 8b-10b scheme as per Widmer and Franaszek. Command channel data transmitted from the DCM to the FEB is synchronous with the Clock channel such that data on the Command channel will transition approximately 90 degrees phase shifted with respect to Clock channel edges. FEBs may use the clock on the Clock channel to capture data on the Command channel and avoid having to recover the clock from the command data stream. Note that data must be captured on both rising and falling edges of the clock. Data on the Data channel arriving at the DCM will be synchronous with the clock channel, but the phase relationship is unknown due to the variable round trip delay in the cable. DCM will recover the clock from the 8b-10b data stream and phase adjust it to allow the serial data to be captured.

On both links, K28.1 characters are used as comma characters. Commas are sent continuously whenever no data is being transmitted. Any non-comma character can be considered a part of a Data or Command Frame. Frames are strings of bytes whose length is fixed for each Frame type. Frame ID codes are used to identify the frame type. Frames take the form of a header followed by a number of payload bytes. Any non-Comma character following a Comma is considered the first byte of a frame. Any number of contiguous Comma characters may be sent between frames. Frames on the Data Channel may be sent contiguously (no comma between frames), but a comma must be sent at least every 1024 characters to verify link synchronization. Commas must not reside in the middle of a frame. Most significant bytes are always transmitted first.

Command Channel Frames

Command Channel Frames have the general form of a one byte header optionally followed by some number of payload bytes. The most significant three bits in the header form the Frame ID field. Valid Command Channel Frame ID codes are shown in Figure 7. The first non-comma character after a comma is considered the first byte of a command frame. Any comma character occurring in the middle of a command frame is considered a frame error. The DCM will wait until it has received all data requested by a command before issuing another command. If requested data is not received after 512 characters a time-out error is declared.

Code	*Function*
0	Send Comma Command
1	Report Status Command
2	Write Register Command
3	Read Register Command

4	Synchronize Clock Command
5	Reserved
6	Reserved
7	Ping Command

Figure 7 Command Channel Frame ID Codes

Send Comma Command Frame

7 *5*	*4* *0*
000	TBD

Figure 8 Send Comma Command Frame Header

The Send Comma Command Frame consists of a one byte Send Comma Command header and no payload bytes. Upon receipt of Send Comma Command Frame, FEB transmits 256 contiguous Comma characters.

Report Status Command Frame

7 *5*	*4* *0*
001	TBD

Figure 9 Report Status Command Frame Header

The Report Status Command Frame consists of a one byte Report Status Command header and no payload bytes. Upon receipt of a Report Status Command, FEB transmits a 10 byte status frame.

Write Register Command Frame

7 *5*	*4* *0*
010	TBD

Figure 10 Write Register Command Frame Header

The Write Register Command Frame consists of a one byte Write Register Command header followed by a four byte payload. The first two bytes of the payload specify the 16-bit address of the register to be written. The third and fourth bytes contain data to be written to the register. The most significant byte is always transmitted first.

Read Register Command Frame

7 *5*	*4* *0*
011	TBD

Figure 11 Read Register Command Frame Header

The Read Register Command Frame consists of a one byte Read Register Command header followed by a two byte payload. The two bytes of the payload specify the 16-bit address of the register to be read. Data from the register addressed is returned to the DCM via the Data Channel in the form of a 16-bit Register Header followed by two bytes of data.

Synchronize Clock Counter Frame

7 5	*4 0*
100	TBD

Figure 12 Synchronize Clock Command Frame Header

The Synchronize Clock Counter Frame consists of a one byte Synchronize Clock Counter command header with no payload bytes. FEB's clock counter is initialized to its programmed preset value upon receipt of the next Sync pulse on the Sync Channel.

Ping Command Frame

7 5	*4 0*
111	00000

Figure 13 Ping Command Frame Header

The Ping Command Frame is used for clock system training. Upon receipt of a Ping Command Frame on the Control Channel, FEB simply returns the Ping Command Frame on the Data Channel. DCM measures the round trip time of the ping to allow it to adjust the clock phase to each FEB. This allows the DCM to synchronize the timing among all 64 FEBs connected to it. Ping commands are only valid if sent while FEB is in Idle mode (Ref: Nathan Felt, et. al.) FEB must ignore Ping commands sent while it is in any other mode.

Data Channel Protocol (FEB to DCM)

Data on the Data Channel is encoded in a similar fashion to that on the Command Channel. 8b-10b encoding is used with comma characters for link synchronization and for frame delineation. Frames may be separated by any number of comma characters as long as at least one comma is sent every 1024 characters to verify link synchronization.

Data Channel Frames

Data on the Data Channel is transmitted in frames. Frames have the general form of a two byte header word optionally followed by some number of payload bytes. The most significant three bits of the header form the Frame ID field. Valid Frame ID codes are shown in Figure 15.

15 13	*12 10*	*9 0*
Frame ID	Seq. Num.	(Frame ID specific)

Figure 14 Data Channel Frame Header

Code	*Function*
0	Empty Frame (no data)
1	Data Frame
2	Status Frame
3	Calibration Frame
4	Register Frame
5	Timing Marker

6	Reserved
7	Ping Echo

Figure 15 Valid Frame ID Codes

All frame headers also have a three bit Sequence Number adjacent to the Frame ID. The frame sequence number is reset on FEB reset and increments by one count for each frame transmitted. The counter wraps to zero upon reaching maximum count. The DCM uses this count as a sanity check to look for missing frames or frames out of sequence. Either of these conditions is considered an error. No effort is made to keep sequence counters synchronized between FEBs.

Empty Frame

Most Significant Byte	*Least Significant Byte*
Data Header High Byte	Data Header Low Byte
Time Stamp Byte 3	Time Stamp Byte 2
Time Stamp Byte 1	Time Stamp Byte 0
Don't Care	Don't Care
Reserved Byte 1	Reserved Byte 0

Figure 16 Data Channel Empty Frame (FEB to DCM)

15 13	*12 10*	*9 5*	*4 0*
001	Seq. Num.	TBD	Pixel Address

Figure 17 FEB Empty Frame Header

Empty frames consist of a 16-bit header word followed by eight bytes of data as defined in Figure 16.

Data Frame

Most Significant Byte	*Least Significant Byte*
Data Header High Byte	Data Header Low Byte
Time Stamp Byte 3	Time Stamp Byte 2
Time Stamp Byte 1	Time Stamp Byte 0
Pulse Height High Byte	Pulse Height Low Byte
Reserved Byte 1	Reserved Byte 0

Figure 18 Data Channel Data Frame (FEB to DCM)

15 13	*12 10*	*9 5*	*4 0*
001	Seq. Num.	TBD	Pixel Address

Figure 19 FEB Data Frame Header

Data frames consist of a 16-bit header word followed by eight bytes of data as defined in Figure 18. Most significant bytes are always transmitted first.

The Data Frame Header consists of a three bit frame ID code, a three bit frame sequence count, a five bit Pixel Address, and 5 TBD bits.

The data portion of the frame follows the header, and is defined as four bytes of time stamp followed by two bytes of pulse height and two TBD bytes.

Data frames transmitted from FEBs are time ordered. A Data frame arriving at the DCM with a timestamp that is earlier than the timestamp on the previous Data frame is considered an error condition. Multiple frames with the same timestamp are allowed, but such frames must have unique pixel addresses.

Upon entering Run DAQ mode, FEBs must wait not send any data frames until after the first time Marker frame has been sent.

Status Frame

Most Significant Byte	*Least Significant Byte*
Status Header High Byte	Status Header Low Byte
Status Byte 7	Status Byte 6
Status Byte 5	Status Byte 4
Status Byte 3	Status Byte 2
Status Byte 1	Status Byte 0

Figure 20 Data Channel Status Frame (FEB to DCM)

15 13	*12 10*	*9 0*
010	Seq. Num.	TBD

Figure 21 FEB Status Frame Header

Status frames consist of a 16-bit header word followed by eight bytes of status information.

Calibration Frame

Most Significant Byte	*Least Significant Byte*
Calibration Header High Byte	Calibration Header Low Byte
Calibration Byte 7	Calibration Byte 6
Calibration Byte 5	Calibration Byte 4
Calibration Byte 3	Calibration Byte 2
Calibration Byte 1	Calibration Byte 0

Figure 22 Data Channel Calibration Frame (FEB to DCM)

15 13	*12 10*	*9 0*
011	Seq. Num.	TBD

Figure 23 FEB Calibration Frame Header

The Calibration Header signifies that a calibration frame of eight bytes follows.

Register Frame

Most Significant Byte	*Least Significant Byte*
Register Header High Byte	Register Header Low Byte
Register Data High Byte	Register Data Low Byte

Figure 24 Data Channel Register Frame (FEB to DCM)

15 13	*12 10*	*9 0*
100	Seq. Num.	TBD

Figure 25 FEB Register Frame Header

The Register Header signifies that a register data frame follows. Two words of data from a register requested by a Read Register Command follow with the most significant word first, and the least significant word second.

Time Marker Frame

Most Significant Byte	*Least Significant Byte*
Time Marker Header High Byte	Timer Header Low Byte
Time Stamp Byte 1	Time Stamp Byte 0

Figure 26 Data Channel Time Marker Frame (FEB to DCM)

15 13	*12 10*	*9 8*	*7 0*
101	Seq. Num.	Reserved	FEB Status

Figure 27 FEB Time Marker Frame Header

The Time Marker character is sent whenever bits n-0 of the FEB's time counter rolls to zero. The number of bits is configurable by writing the Time Marker Mask bits in the FEB during initialization. Upon entering Run DAQ mode, the FEB must not send any data frames until the first Time Marker Frame has been sent.

Ping Echo Frame

Most Significant Byte	*Least Significant Byte*
Ping Echo Header High Byte	Ping Echo Header Low Byte
Reserved	Reserved

Figure 28 Data Channel Ping Echo Frame

15 13	*12 10*	*9 0*
111	Seq. Num.	FEB Status

Figure 29 FEB Ping Echo Frame Header

The Ping Echo Frame consists of a two byte header with two payload bytes. It is transmitted by FEB upon receipt of a Ping Command Frame from DCM when FEB is in Idle mode. A Ping Command Frame is ignored by the FEB if it is not in Idle mode.

Initialization and Operation

On power up, all channels will remain static (undefined levels) until board initialization is complete. Once DCM initialization completes, it will drive Sync to its negated level, start driving Clock with the front end clock frequency, and begin transmitting Idle characters on the control channel. DCM then monitors the Data channel attempting to capture idle characters transmitted from the FEB. FEB remains quiet on the Data channel until it begins receiving Idle characters from the DCM. Once FEB recognizes IDLE characters on the Command channel, it begins transmitting Idle characters on the Data channel. FEB disables its Data channel driver whenever it is unable to decode valid characters on the Command Channel.

References

1. ANSI/TIA/EIA-568-B.1-2001. "Commercial Building Telecommunications Cabling Standard - Part 1: General Requirements".

2. ANSI/TIA/EIA-568-B.2-2001. "Commercial Building Telecommunications Cabling Standard – Part 2: Balanced Twisted Pair Cabling Components".

3. ANSI/TIA/EIA-644-A-2001. "Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits".

4. X. Widmer and P. A. Franaszek. "A DC-Balanced, Partition-Block, 8B/10B Transmission Code". IBM Journal of Research and Development, 1983: Volume 27, Number 5, Page 440.

5. Nathan Felt and John N. Oliver. "FEB Control", Nova Doc 865, 15 May 2006.